Ultra-Low-Voltage LNA with High Gain and Low Noise Figure

Ivan Bastos, Luis B. Oliveira, João P. Oliveira, João Goes, and Manuel M. Silva

***Abstract*—We present a balun LNA with noise and distortion cancellation using double feedforward. A common-gate and a common-source stage are combined, and their resistive loads are replaced by transistors biased close to saturation to allows low supply voltage, without gain degradation. The proposed feedforward boosts the LNA gain and reduces the noise figure (NF). Simulation results with a 130 nm CMOS technology show that the gain is up to 24 dB and the NF is below 3.2 dB. The total power dissipation is 2.25 mW, leading to an FoM of 6.4 mW^{-1} with 0.6 V supply.**

***Index Terms*—LNA; CMOS; noise cancellation**

I. Introduction

THE present high demand for wireless communications includes Industrial, Scientific, and Medical (ISM) and Wireless Medical Telemetry Service (WMTS) applications [1]. These require low power, low voltage transceivers, which can be fully integrated in a single chip [2-4], to reduce the area and cost. A key block in these systems is the LNA, which is investigated in this paper.

Recently, wideband LNAs with high gain and low noise figure, using noise and distortion cancelation have been proposed [5-7]. However, these circuits cannot operate with low voltage, to avoid performance deterioration.

In this paper, our main goal is to design a very low area and low cost LNA, operating at 0.6 V supply with high gain and low noise figure. The proposed circuit is, as far as we know, the first wideband LNA with noise and distortion cancellation capable to operate at 0.6 V. This is obtained by replacing the load resistors by transistors biased close to saturation.

In [7], a circuit operating at 1.2 V with controllable gain was proposed. In this paper we investigate the possibility of using this circuit at 0.6 V and introduce a double feedforward technique to boost the gain and reduce the noise figure.

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Equations for gain and noise figure are presented, which can be used to optimize the circuit performance. Circuit prototypes in a 130 nm standard CMOS technology at 1.2 V and 0.6 V have been designed and simulated to demonstrate the proposed techniques.

The circuit prototype at 0.6 V has gain of 23.9 dB and NF below 3.2 dB, dissipating only 2.25 mW, leading to a FoM of 6.4 mW^{-1}, which is, to the authors' knowledge, the best FoM in the literature.

In section II we describe the conventional balun LNA. In section III we present the proposed solution to increase gain and reduce NF. In section IV we present the simulation results for the two circuit prototypes. Finally, in section V we draw the conclusions.

II. Balun LNA with Noise Cancellation

In a receiver, the antenna and RF filter are usually, single-ended, so a balun LNA is required to perform a single-ended to differential conversion, thus avoiding the traditional external balun circuit, which has significant loss, and degrades the NF. An LNA differential output has the advantages of reduced harmonic distortion and good power supply and substrate noise rejection.

The circuit proposed in [6] and shown in Fig. 1 is a balun LNA, in which the thermal noise of M_1 (main source of noise) is cancelled out. The noise produced by M_1 appears in phase at the two outputs terminals, while the signals at these terminals are in opposition. Thus, the gain is doubled and the noise is cancelled. It can be shown [6] that the distortion introduced by M_1 is also cancelled.

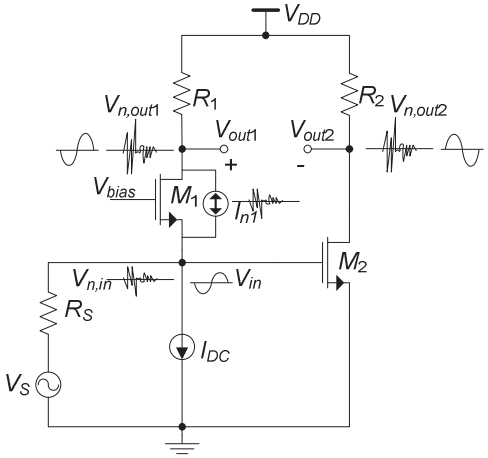

Figure 1. Balun LNA with noise canceling [6].

The differential voltage gain of the LNA is obtained from the gain of a common-gate (CG) stage plus the gain of the common-source (CS) stage:

$$A_v = g_{m1}R_1 + g_{m2}R_2 \quad . \tag{1}$$

As shown in [6], the gains of the two stages should be equal for balanced balun operation and for noise and distortion cancellation. The maximum gain is limited by the value of the resistors since g_{m1} is responsible for the input matching.

The circuit in Fig. 1 cannot operate at 0.6 V with high gain, due to the large voltage drop in the resistors. In this paper, we propose a solution to overcome this limitation: we replace the resistor loads by transistors and we apply a double feedforward technique to increase the gain and reduce the noise figure.

In recent years several circuits have been proposed having in common the noise cancellation, gain boosting or a combination of both techniques. The advantages and disadvantages of each circuit are summarized in Table I.

The main motivation for this paper is to achieve a LNA design that can be able to maintain the main key advantages of the circuits presented in Table I, and overcome some of the disadvantages (low gain and high NF).

TABLE I.
COMPARISON OF STATE-OF-THE ART LNAS

LNA	Advantages	Disadvantages
[6]	balun operation circuit simplicity noise and distortion cancellation good linearity wide bandwidth	high sensitivity to dc bias sensitivity to PVT variations limited gain
[8]	balun operation low voltage operation low power flexible design	reduced bandwidth linearity dependence on dc bias
[9]	partial noise cancellation very low noise figure good linearity	differential input (not balun) limited bandwidth high power consumption circuit complexity
[10]	high voltage gain very low power	differential input (not balun) circuit complexity limited bandwidth poor linearity

III. PROPOSED CIRCUIT

In the proposed LNA circuit, a double feedforward structure is used, as shown in Fig. 2, in order to boost the gain.

Since the g_{m1} value is set by the 50 ohm input matching, to boost this stage gain we must use the load. First, we replace the resistors by transistors close to saturation, and then we apply feedforward using an inverter gain block with gain α between -1 and -4 (inversion is required, since the CG stage does not change the signal phase). The overall gain is boosted by the combination of active loads and feedforward.

For the common-source stage, this feedforward is simpler: since g_{m2} can be changed, a simple feedforward without voltage gain can be used (simulations have shown that there is no advantage in adding a gain block in this feedforward loop).

We derive equations for the gain. First, we consider transistors as active loads, without feedforward:

$$A_v = g_{m1}(r_{o1}//r_{o3}) + g_{m2}(r_{o2}//r_{o4}) \; . \tag{2}$$

Then, for the circuit of Fig. 2, we must include in the previous equation the gain boosting due to the double feedforward:

$$A_v = g_{m1}(r_{o1}//r_{o3}) + |\alpha| g_{m3}(r_{o1}//r_{o3}) + \left(g_{m2} + g_{m4}\right)(r_{o2}//r_{o4}) \quad . \tag{3}$$

As in [6, 7], if we assume that $g_{m1} = g_{m2} = g_m$, then the noise factor without feedforward is

$$F_{LNA} = 1 + \frac{k_f}{8kTR_S c_{ox} f^{\alpha f}}\left(\frac{1}{W_1 L_1} + \frac{1}{W_2 L_2}\right) + \frac{\gamma}{2R_S g_m} + \frac{1}{R_S r_{op} g_m^2}, \tag{4}$$

where k is Boltzmann's constant, c_{ox} is the oxide gate capacitance per unite area, W_i and L_i are the transistor dimensions, T is the absolute temperature, γ is the excess noise factor, k_f and α_f are intrinsic process parameters, which depend on the size of the transistors [11, 12]. With feedforward (Fig. 2) there is the additional noise of the feedforward amplifier, but this can be minimized by proper design.

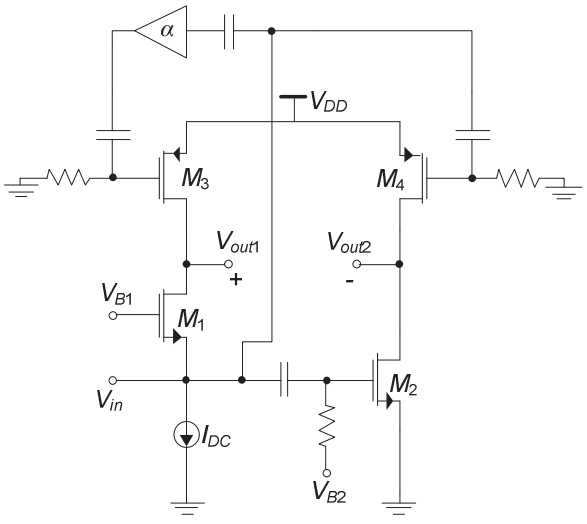

Figure 2. Proposed LNA.

IV. SIMULATION RESULTS

Two circuit prototypes are designed using a 130 nm CMOS standard technology, the first prototype with 1.2 V supply voltage and the second with 0.6 V supply.

In the LNA prototype with 1.2 V supply, the transistors have W_1 = 67.2 µm, W_2 = 115.2 µm and $W_3 = W_4$ = 12.4 µm.

For maximum speed, all transistors have the minimum channel length (120 nm). The current source that bias the CG stage is set to 2 mA and the gain block is an inverter based amplifier with resistive feedback self-bias [13].

For the LNA prototype with 0.6 V supply, the transistors widths are W_1 = 80 µm, W_2 = 92.8 µm and W_3 = 48 µm and W_4 = 57.64 µm. For maximum speed, all transistors have the minimum channel length (120 nm). The current source that biases the CG stage is set to 1.35 mA, and the gain block is a inverter based amplifier using a dynamic threshold MOS (DTMOS) structure [14], in order to reduce the resistive noise contribution and also to better cope with the low voltage supply requirements.

In table II we compare the simulation results with the theoretical values. For comparison, we also consider the conventional case with 200 Ω resistors [6]. We can observe that the simulations agree with the theory.

TABLE II.
OPTIMIZED GAIN (DB) FOR DIFFERENT TOPOLOGIES AND VOLTAGE SUPPLY 1.2 V AND 0.6 V

	Vdd	Resistor load	MOSFET load	with FF (α = -1)	with FF (α = -4)
Theoretical	1.2 V	18.3	19.8	20.5	22.2
Simulation		18.1	19.7	20.3	21.9
Theoretical	0.6 V	11.9	18.7	21.3	24.1
Simulation		11.7	18.5	21.1	23.9

In order to investigate the influence of feedforward in the circuit key parameters, gain, bandwidth, noise figure, and linearity, simulation results are presented in tables III and IV. Four cases are considered: resistor loads (200 Ω), and MOS transistor loads without feedforward; and with double feedforward with gain -1 or -4 in the common-gate stage and 1 in the common-source stage.

The following figure of merit is used [15] in the comparison:

$$FoM[\mathrm{mW}^{-1}] = \frac{Gain}{(F-1)P_{DC}[\mathrm{mW}]} \quad . \tag{5}$$

In tables III and IV circuit simulation results are presented for 1.2 V and 0.6 V supply voltage, respectively. Table III shows that with 1.2 V, there is a significant increase of the gain, without a penalty in the NF, in comparison with the resistive loads. This is also shown in Figs. 3 and 4. The disadvantages are the increase of circuit non-linearity and a reduction of the available bandwidth. The FoM is similar for the different cases, but with some advantage for the active load circuits when compared with resistive load circuits.

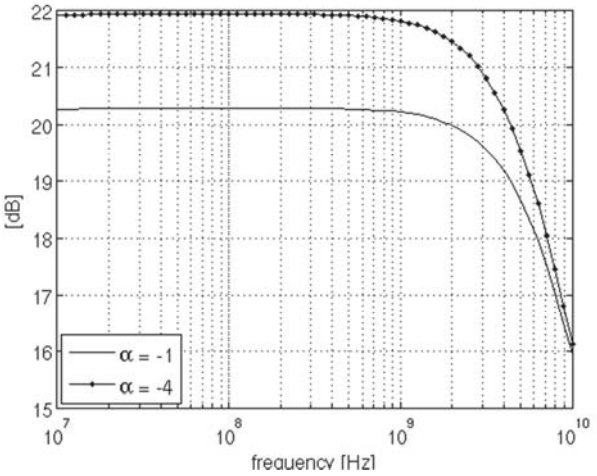

Figure 3. Gain simulations for the prototype with 1.2 V supply.

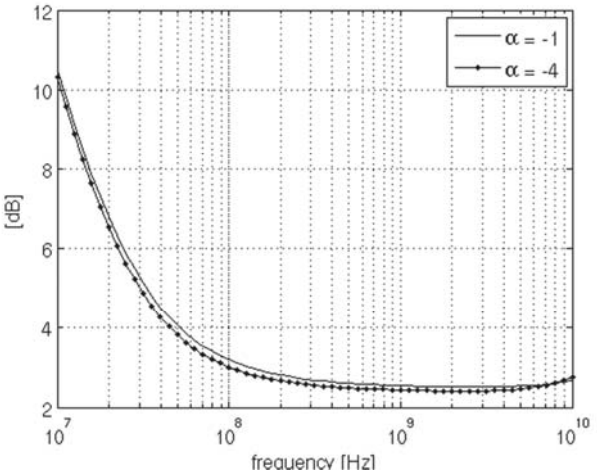

Figure 4. NF simulations for the prototype with 1.2 V supply.

TABLE III.
CIRCUIT SIMULATIONS FOR 1.2 SUPPLY.

	BW (GHz)	Av (dB)	NF (dB)	IIP3 (dBm)	PDC (mW)	FoM (mW^{-1})
Res	0.1-10.8	18.1	< 3.1	10.2	5.1	1.5
MOS	0.1-7.7	19.7	< 2.8	-3.3	4.9	2.1
FF α=-1	0.1-7.4	20.3	< 3.2	-4.2	5.4	1.7
FF α=-4	0.1-5.9	21.9	< 3	-8.6	6.2	2.0

TABLE IV.
CIRCUIT SIMULATIONS FOR 0.6 SUPPLY

	BW (GHz)	Av (dB)	NF (dB)	IIP3 (dBm)	PDC (mW)	FoM (mW^{-1})
Res	0.1-10	11.7	< 4.1	7.7	1.9	1.3
MOS	0.1-4.8	18.5	< 2.9	-9.5	1.8	4.9
FF α=-1	0.1-3.4	21.1	< 3	-16.7	2.1	5.4
FF α=-4	0.1-1.3	23.9	< 3.2	-26	2.25	6.4

The circuit prototype operating at 0.6 V has similar performance in terms of gain and NF, when compared with the circuit operating at 1.2 V, as shown in Figs. 5 and 6, but there is a strong reduction of power consumption, which leads to the best FoM (Table III). With 0.6 V, the LNA with resistors has poor performance, since the value of the resistances must be strongly reduced to avoid a large voltage drop.

When comparing the simulation results with those in the literature, we observe that our circuit is very good in terms of gain and NF, and has very low power. This leads to the best FoM (since the results are obtained by simulation, some degradation is to be expected in the fabricated circuit; some of the results in table V are obtained by measurement).

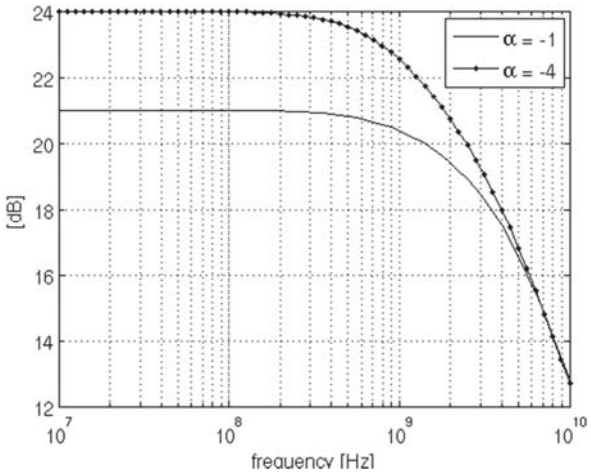

Figure 5. Gain simulations for the prototype with 0.6 V supply.

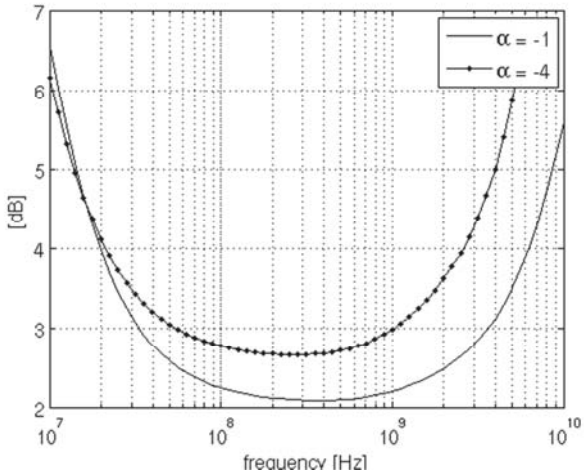

Figure 6. NF simulations for the prototype with 0.6 V supply.

The proposed approach is especially interesting in low power and low voltage biomedical applications [1], since in these applications low power is essential, but some non-linearity can be tolerated (usually, the target application only needs a low data rate communication link). There are ISM bands at 450 MHz and 900 MHz and a WMTS band at 600 MHz, for which this circuit can be a good alternative to the conventional solutions.

TABLE V.
COMPARISON WITH STATE OF THE ART LNAS.

	Tech (nm)	Band (GHz)	Gain (dB)	NF (dB)	Power (mW)	FoM (mW^{-1})
[6]	65	0.2-5.2	13-15.6	< 3.5	14	0.4
[9]	90	0.1-2.3	21	<1.7	18	1.3
[16]	90	0.5-8.2	22-25	< 2.6	42	0.5
[17]	90	0.8-6	18-20	< 3.5	12.5	0.6
[18]	90	0.1-1.9	20.6	< 2.7	9.6	1.3
[19]	130	0.2-3.8	11.2	< 2.8	1.9	2.1
[8]	130	0.2-3.8	19	<3.4	5.7	1.3
[10]	130	0.1-2.7	20	<4	1.3	5
[20]	180	0.5-0.9	16	<4.3	22	0.2
[21]	180	0.1-0.9	15	< 4.2	10	0.3
This Work (α=-4)	**130 (1.2V)**	**0.1-5.9**	**21.9**	**<3**	**6.2**	**2.0**
This Work (α=-4)	**130 (0.6V)**	**0.1-1.3**	**23.9**	**<3.2**	**2.25**	**6.4**

V. CONCLUSIONS

In this paper we present a low voltage and low power wideband balun LNA with double feedforward for high gain and low noise figure. Two circuit prototypes operating at 1.2 V and 0.6 V are presented in a 130 nm CMOS technology, which validate the proposed methodology. Simulation results show that the gain of the balun LNA, operating at 0.6 V is enhanced to 24 dB, and the NF is below 3.2 dB for a power consumption of 2.25 mW. The proposed circuit is especially useful for low power and low voltage operation in biomedical applications (ISM and WMTS).

The proposed circuit, with 0.6 V supply, to the best of the authors' knowledge, has the higher FoM (6.4 mW^{-1}) when compared with CMOS LNAs in the literature.

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Prof. Goes has supervised 7 Ph.D. and 14 M.Sc. theses, and he has published over 100 papers in international IEEE Journals and leading Conferences, and he is co-author of 5 books.

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He is the author of two textbooks on circuit theory and electronic circuits, which are widely used in Portuguese Universities and Polytechnic Institutes.
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