A 1.25GS/s 12bit and 2.27mW Digital to Analog Converter (DAC) with 70.22 SNDR Based on New Hybrid R-C Procedure in 180nm CMOS

Sina Mahdavi, Maryam Poreh, Leyla Alizadeh, Baran Moradkhani, and Rezvan Ebrahimi

***Abstract*—This paper presents a novel fully differential high-speed and high-resolution Digital to Analog Converter (DAC) based on new reliable hybrid R-C technique. In the proposed idea the four LSB bits and eight MSB bits are implemented as a resistor string and new merged capacitor technique respectively. Applying the suggested method the SNDR and Effective Number of Bits (ENOB) of the proposed DAC achieve 70.22dB and 11.41bit at the 1.25GS/s sampling rate correspondingly. In the proposed method the total capacitors of the 8 MSB bits are reduced up to 78% compared to the conventional one noticeably. As a result, the power consumption and speed of the suggested DAC are decreased and increased respectively. Moreover, the total power consumption of the proposed DAC is 2.27mW with the power supply of 1.8 volts as well. Meanwhile, for the correctness of the proposed 12bit DAC, 200 iterations in transient Monte-Carlo analysis (parasitic capacitance included ($\partial_{mismatch} = 1.2\%$)), and the SNDR simulation results versus different input frequency at fS=1.25GS/s sampling rate are applied too. The maximum Integral Nonlinearity (INL) and the maximum Differential Nonlinearity (DNL) are -0.47/+0.35LSB and -0.42/+0.29 LSB respectively. The proposed DAC structure is simulated in all process corners and performed using the HSPICE BSIM3 model of a 0.18µm CMOS technology.**

***Index Terms*—SAR ADC, DAC, High-resolution, Power consumption, High-speed**

I. Introduction

DIGITAL to Analog Converters (DACs) are usually used in a medical instrument for converting pulses from discrete sample to continuous analog waveform, mixed mode integrated circuits [1, 2, 3, 4, 5, 7, 22, 23, 24, 27]. Considerably, current-string DAC were preferred for many years [10, 16, 18, 24, 25], however, due to large layout dimensions, such design is very sensitive in both to device mismatch and to local deterministic disturbances also known as gradient error [24, 26]. It is notable that, this drawback becomes more significant with an introduction of nanometer technologies [5, 7, 8, 9, 14, 21, 24]. Different DAC structures have been designed with various advantages and disadvantages. R-2R ladder DAC, Binary weighted DAC, current steering DAC and resistor string DAC are the most common DACs that are used in many applications [5, 14, 15, 18].

In the resistive type DACs, the resolution was restricted because of mismatches. Also, they need additional buffers for driving purposes, and they should be customized depending on applications as their supply voltage varies [1, 22, 23, 25, 27]. While Current-steering DAC is widely used in the modern communication standards. Thermometer-coded DAC is often used in the high-linearity system [7, 24-27]. Meanwhile, thermometer-coded DAC operates by dividing each N bit into the 2N quantity of current sources, which are controlled one by one in accordance with the data transmission [14, 15, 16, 22, 26]. This approach makes the glitches smaller and lowers the DNL. However, this approach usually requires a relatively big area of the chip due to large decoding circuits. Binary-weighted DAC, on the other hand, directly use the binary code to control the weighted current sources. While this implementation does not require additional decoding circuit, it will relatively lead to a bigger glitch and worsen the DNL performance. In addition, the slight output impedance of higher-order weighted current sources will affect the linear system [1, 5, 10, 13, 22, 26]. For instance, it is well-known that the digital to analog converter is one of the most significant blocks in the SAR ADC architectures, a capacitive DAC is used in the conventional SAR ADC due to its good matching and power efficiency usually [11, 12, 13, 18]. However, the number of unit capacitors in DAC increases exponentially as the number of bit increases, a DAC block occupies the largest area among many internal blocks in a SAR ADC [2, 10, 11]. To reduce the number of unit capacitors, a split-capacitor DAC is commonly used. On the other hand, the parasitic capacitances and mismatch associated with the bridge capacitor along with the mismatches of the binary weighted capacitor arrays reduce the linearity of the internal DAC noticeably [2, 10, 11, 18]. Recently, to improve the linearity of split-capacitor DAC, calibration techniques have been proposed but it requires extra hardware, more power consumption and large area [2, 6, 11, 12, 13]

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Basically, C-2C DAC technique is another choice to achieve high-speed and moderate resolution [16, 20]. It is notable that, a C-2C DAC has some major advantages related to its binary weighted counterpart [17, 28]. For instance, the capacitive input loading is fixed and the DAC size increases linearly with the resolution, as a result the bandwidth is larger. [19, 28]. Conversely, the parasitic capacitance problem in the C-2C DAC causes an accuracy limitation and it is hard to achieve high resolutions with this topology [16-20].

Hybrid architecture is another of segmented methods to extend the resolution of a DAC through combining different types of sub- DACs together. Segmented methods are widely used in parallel DACs, such as resistor-string DACs and current steering DACs and capacitive DAC when their resolution is high [3, 13]. The major category of hybrid segmented DACs is resistor-capacitor hybrid type since the resistor-capacitor hybrid method is to scale the analog output or the reference voltage of the LSB sub-DAC and add this scaled voltage with the output voltage of the MSB sub-DAC [11, 12, 13, 22].

In this paper, to enhance the resolution and the speed of the DAC structure simultaneously, a novel fully differential merged R-C technique is presented. Meanwhile, the power consumption of the proposed DAC is low compared to the conventional one. The proposed paper is organized as follows. In section II the proposed DAC structure is discussed. Simulation results are presented in section III, and finally, section IV concludes the paper.

II. The Proposed Fully Differential DAC Structure

Fig. 1 indicates the old-style structure of the 12-bit charge-redistribution capacitor arrays. Where the capacitors consensus to the following proportion: 1:1:2:4:8:16…512:1024:2048 [2, 4, 10, 11, 18, 23].

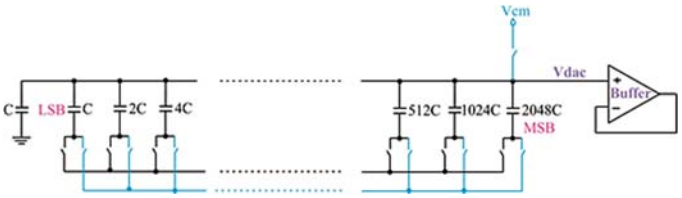

Fig. 1. A 12-bit conventional capacitor DAC

Therefore, in the conventional structure of capacitor array, the number of the capacitors increases exponentially with the increase of DAC effective number of bits, for instance, in the 12-bit resolution DAC, the Most Significant Bit (MSB) capacitor is 2048 times larger than compared to the Least Significant Bit (LSB) capacitor, it is unrealistic for a high-precision and high-speed DAC obviously [2, 4, 9, 10, 11, 12, 13, 18]. On the one hand, due to the large capacitors array, the chip area is increased too. Meanwhile, mismatch effect between the capacitors become larger with the increase of the capacitance and the error will also increase. So, the capacitor array segmented structure has been widely used, but the linearity of DAC will decrease, because of the introduction of the match-capacitor in this structure. A resistor string DAC can be used to avoid these drawbacks which offer high-speed operation and small area compared to charge-redistribution capacitive DAC [9, 11, 12, 18]. However, it causes large DNL errors and hardly achieves good INL which limits their resolution owing to the switch resistance between resistors strings array [7, 8, 11, 12]. Equation (1) indicates the 12 bit capacitor DAC output voltage, where Vref, Cp and a1 are the reference voltage, parasitic capacitor and digital codes of the first bit respectively [10].

In order to overcome the mentioned problems in both of the conventional charge–redistribution and resistor string DAC array, a novel merged method is implemented in this paper to achieve high-speed and high-resolution DAC simultaneously. The schematic diagram of the fully differential proposed 12-bit DAC is depicted in Fig. 2. As it is clear, it consists of a 4-bit (LSB bits) resistor array, 4-bit C-2C capacitive technique, and 4-bit (MSB bits) charge redistribution capacitive array.

$$Vdac = \frac{a1*C*Vref}{2C+Cp} + \frac{a2*\frac{C}{2}*Vref}{2C+Cp} + \cdots + \frac{a12*\frac{C}{4096}*Vref}{2C+Cp} \quad (1)$$

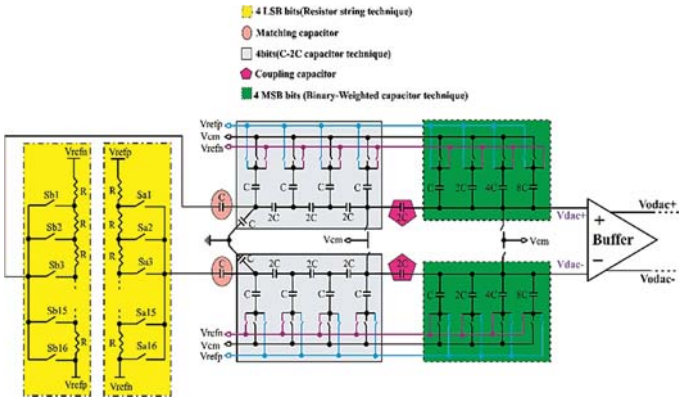

Fig. 2. The proposed 12bit DAC structure

The resistor string DAC's output is connected to the 8-bit capacitor DAC through the matching capacitor. Then the resistor string DAC is used only for the 4 LSB bits, in the low four bits, resistor divider configuration uses a series of resistors which have the same resistance value to divide the reference voltage into 16 parts equally, the output of these voltages is controlled by 16 switches respectively, the resistance of a unit resistor is considered 600 ohm. The matching requirement of the unit resistor is relaxed by a factor of 2^8 compared to the matching of the capacitors. Also, the total number of the unit capacitors is reduced by a factor of 2^4 rather than the conventional capacitive DAC by applying the 4-bit resistor string DAC. It is notable that, Vrefp, Vrefn and Vcm are the maximum reference, minimum reference and common mode voltage of the DAC, and in the proposed idea the total capacitance is reduced noticeably related to the conventional one. For instance, in the suggested merged method the total capacitors of the 8bits (MSB bits) are just 58 unit capacitor, while in the conventional method it requires 510 unit capacitor in order to convert the digital codes to the analog voltage. It means that, in the proposed method the total capacitors of the 8 MSB bits are reduced 78% compared to the conventional one. As a result, the power consumption and speed of the suggested

DAC are decreased and increased respectively. Meanwhile, the C-2C technique is applied to reduce the total capacitance and increase the speed, it is considered that, as simulation results prove, the effects of the parasitic capacitors in C-2C DAC are almost negligible in the proposed structure, because just 4bits are implemented C-2C DAC technique. Also, for better matching of the structure, the size of the matching and coupling capacitors are considered C and 2C respectively, also the size of the unit (C) capacitor is chosen 30fF as well.

Fig. 3 shows the differential cascode-driver source-follower buffer [10, 29].

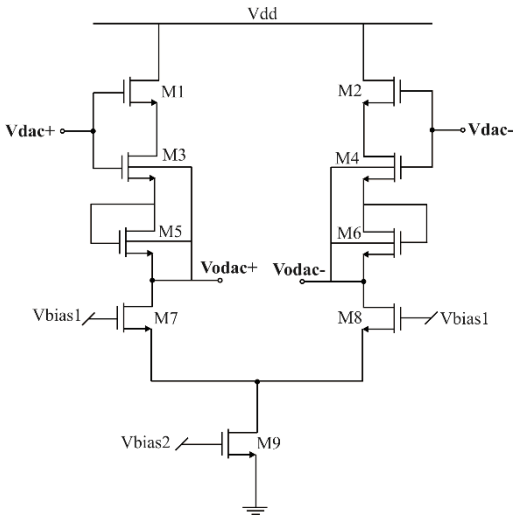

Fig. 3. A differential cascode-driver source-follower buffer

As it is clear in Fig. 3 in this buffer the driver devices (M1-M4) are cascoded. To achieve the main advantage of the cascoded driver, all devices M1-M4 must be remained in saturation region [29]. Also, the function of M5, M6 is the shift in threshold voltages of M3, M4 [10, 29]. Meanwhile, this shift is created by body effect due to source-drain (source-gate) voltage of M5, M6 which is fixed due to a fixed current, in fact the threshold voltage remain fixed as well [29]. The devices of M7-M9 are the current sources of the buffer. Also, Vdac+, Vdac- and Vodac+, Vodac- are the input and output nodes of the buffer respectively.

III. Simulation Results

The simulation results of the proposed DAC are presented in this section. Fig. 4 and 5 show the output Fast Fourier Transform (FFT) spectrum of the suggested DAC with and without considering effect of the parasitic capacitors of C-2C DAC respectively, it is clear that in mentioned Figs, the output Total Harmonic Distortion (THD) is near -71dB and the effect of the parasitic capacitors are almost negligible in the LSB bits C-2C DAC technique. Meanwhile, in the proposed DAC, applying a Nyquist input (623.77MHz sinusoidal input frequency) at 1.25GS/s sampling rate the Signal to Noise and Distortion Ratio (SNDR) and ENOB of the DAC achieve 70.22dB and 11.41bit respectively. Also, the output FFT spectrum of the buffer and its effects in the proposed DAC with Nyquist input at fS=1.25GS/s and considering the effect of the parasitic capacitors in the LSB bits C-2C DAC is indicated in Fig. 6. Double-tone simulation results with the sinusoidal input frequency in 155MHz and 157.5MHz at 1.25GS/s sampling rate is exposed in Fig. 7 noticeably. In the meantime, the capacitors are extracted from a layout and the effect of the parasitic capacitance are considered in the simulations, also, 200 times Monte-Carlo simulation results (parasitic capacitance included ($\partial_{mismatch} = 1.2\%$)), of the behavioral model of the suggested design are shown in Fig. 8, the minimum, mean and maximum SNDR of the proposed DAC is almost 64dB, 70dB and 76dB correspondingly. Fig. 9 summarizes the simulation result of the SNDR versus input frequency with Nyquist (623.77MHz) input, at the sampling rate of 1.25GS/s, the SNDR of the proposed architecture achieves nearly 69dB as well. As shown in Fig. 10 and Fig. 11 the maximum INL and the maximum DNL are -0.47/+0.35LSB and -0.42/+0.29 LSB respectively.

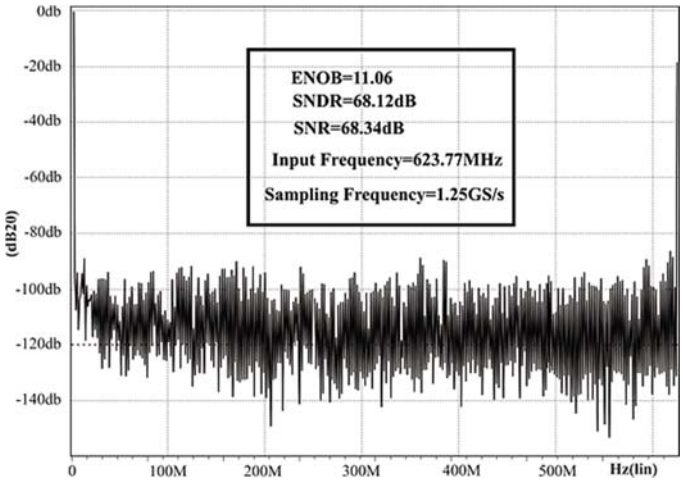

Fig. 4. The output FFT spectrum of the proposed DAC in Nyquist input (fin=623.77MHz) at fS=1.25GS/s with considering the effect of the parasitic capacitors in the LSB bits C-2C DAC

The total power consumption of the suggested DAC is 2.27mW with the power supply of 1.8 volts. Simulation results of the proposed DAC are performed using the BSIM3 model of a 0.18µm CMOS process with the power supply of 1.8volts.

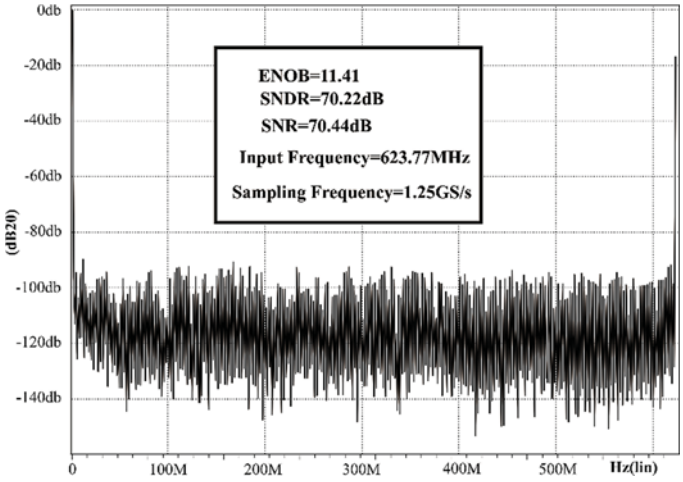

Fig. 5. The output FFT spectrum of the proposed DAC in Nyquist input (fin=623.77MHz) at fS=1.25GS/s without considering the effect of the parasitic capacitors in the LSB bits C-2C DAC

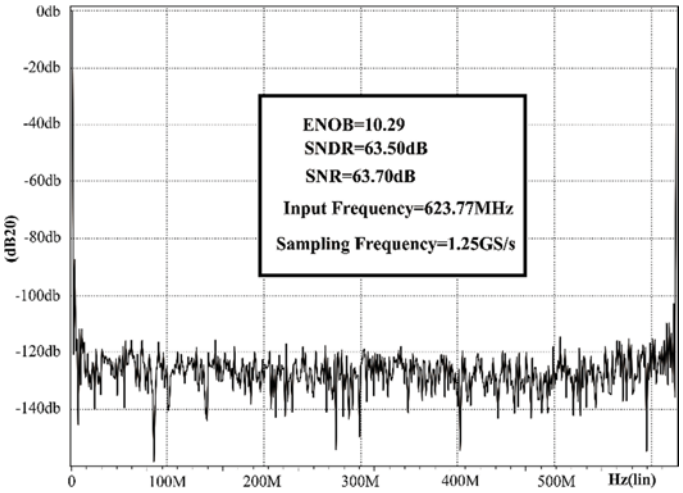

Fig. 6. The output FFT spectrum of the buffer and its effects in the proposed DAC with Nyquist input (fin=623.77MHz) at fS=1.25GS/s and considering the effect of the parasitic capacitors in the LSB bits C-2C DAC

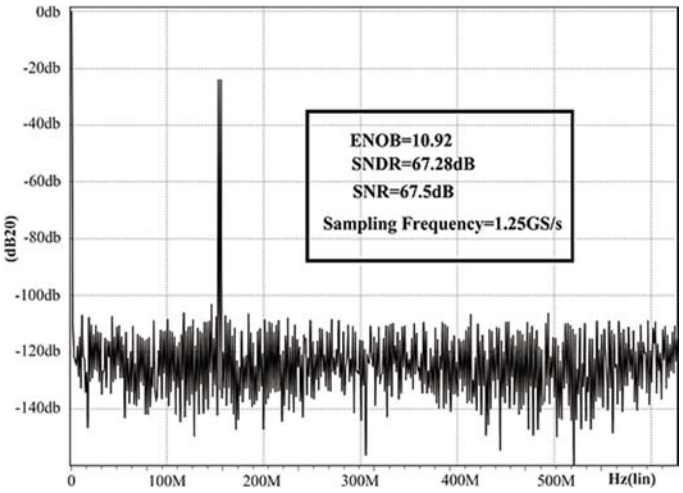

Fig. 7. The double–tone output FFT spectrum of the proposed DAC in fin=155MHz and fin=157.5MHz at fS=1.25GS/s

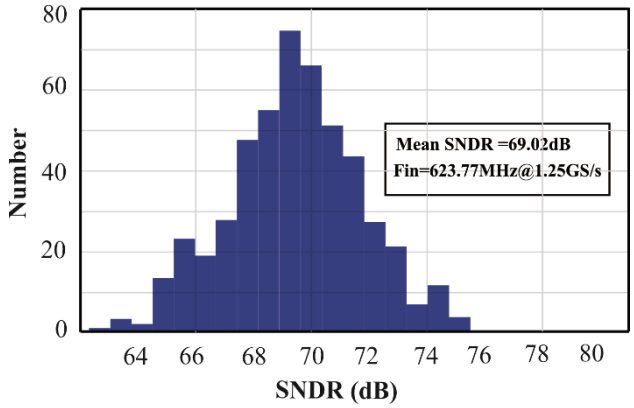

Fig. 8. 200 Monte-Carlo SNDR simulation results of the proposed DAC with Nyquist input at fS=1.25GS/s

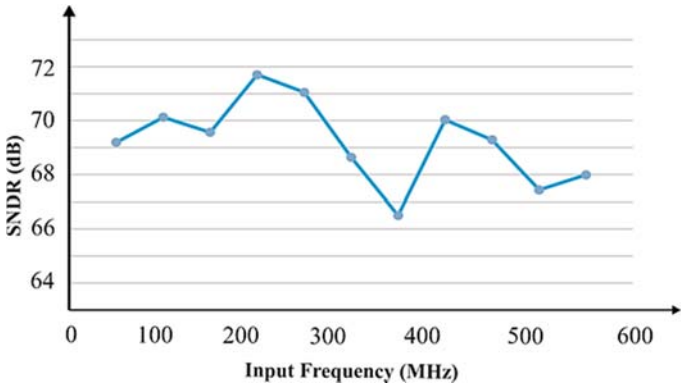

Fig. 9. The SNDR simulation results of the proposed DAC versus different input frequency at fS=1.25GS/s

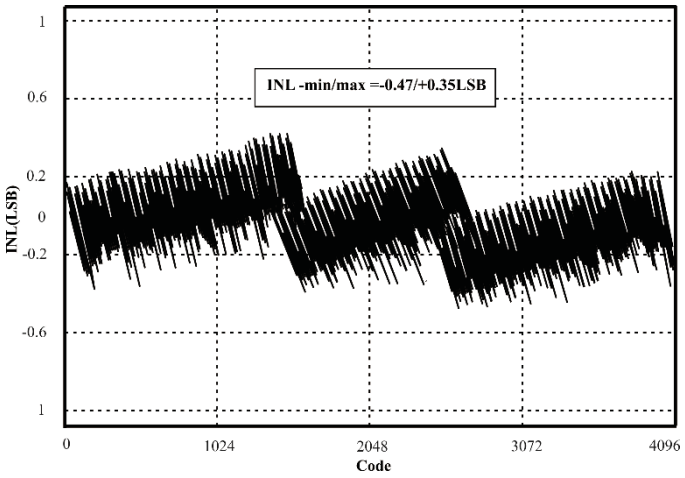

Fig. 10. Simulation result of INL plot

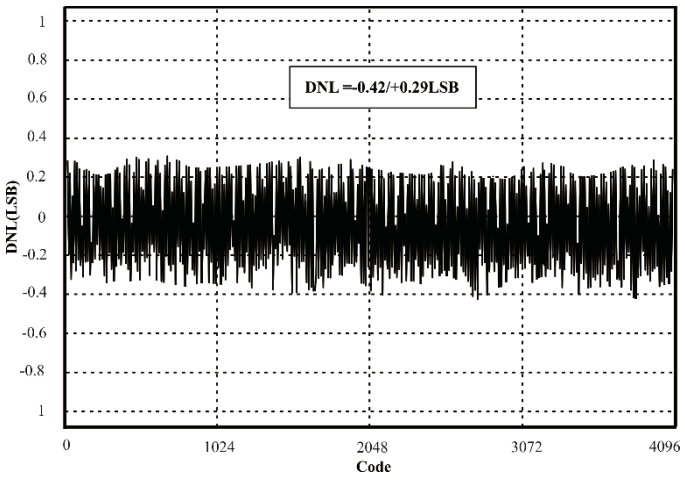

Fig. 11. Simulation result of DNL plot

IV. Conclusions

This paper presents a novel fully differential high-speed and high-resolution Digital to Analog Converter (DAC) according to new reliable merged technique. In the proposed idea the four LSB bits and eight MSB bits are implemented resistor string and new merged capacitor technique respectively. Applying the suggested method the SNDR and Effective Number of Bit

(ENOB) of the proposed DAC achieve 70.22dB and 11.40bit at the 1.25GS/s sampling rate correspondingly. Moreover, the total power consumption of the proposed DAC is 2.27mW with the power supply of 1.8 volts as well. Finally, Table 1 compares this work with the similar previous ones. The proposed DAC structure is simulated and performed using the HSPICE BSIM3 model of a 0.18µm CMOS technology.

TABLE I.
COMPARISON TABLE

Specifications	[1]*	[5]*	[7]*	[22]*	**This****
Technology (nm)	130	40	140	180	180
Resolution (bits)	14	12	14	12	12
Sampling Rate (GS/s)	0.5	1.6	0.2	0.02	1.25
Supply Voltage (V)	1.2/2.5	0.8	1/1.8	1.35	1.8
Power Consumption (mW)	299	40	270	1.74	2.27
SNDR (dB)	>50	-	-	-	70.22
Power supply noise (mW)	-	-	-	-	50
INL/DNL (LSB)	4.5/2.5	-	1.8/2, 3.2/2	7.55/638	-0.47/-0.42
SFDR (dB)	73.5	74	>73	-	-

*Fabrication
**Simulation

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