

High-voltage SoI Unity-gain Voltage Buffers with Function-enable and Power-down Functionality

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Abstract—This paper discusses possibilities of enable and power-down functionality implementation in HV SoI unity-gain buffers. Modifications of selected HV buffer structures are analyzed. Approaches of power-down, high input and output impedance functionality implementation are introduced and discussed.

Index Terms—High-voltage integrated circuits; SoI process; high impedance state; enable functionality

I. INTRODUCTION

OPERATION limiting and power-dissipation cutting functionality as often referred to as “enable/disable” and “power-down” abilities. These functionalities may have quite distinct implementations in electronic circuits. Power-down provides power consumption reduction by shutting down parts or whole function block. Enable/disable functionalities rather tend to stop circuit operation while keeping it fully powered for fast regaining the proper operation. The latter functionalities may also ensure high input/output impedance (Z) in specific states of circuit operation. The design requirements required by specific functionalities may significantly differ. Due to this, design techniques and topologies may become different. The paper presents interesting implementations of the mentioned functionalities into practically used HV unity-gain buffers designed in Silicon on Insulator (SoI) process.

II. THE UNITY-GAIN BUFFER TOPOLOGIES

Unity-gain buffers are widely used in low- and high-voltage integrated circuits (ICs) for signal conditioning and buffering purposes. In case of HV ICs such buffers are usually based on source-follower and gate-follower topologies [1]. HV implementations of these topologies are significantly simpler than in case of HV operational amplifiers (OPAMPs). The unity-gain followers are especially useful in their complementary versions, presented in Fig. 1. Such buffers are used in various applications [2]. Diverse derivatives of source-follower based HV buffers [3, 4] are sometimes used in HV ICs, because of satisfactory voltage gain and low input-output voltage shift levels.

Buffers based on gate-follower structures are less common. They have inherent problem with both voltage gain and input-output voltage shift. These drawbacks may be overcome with specially devised auxiliary control [5], though the buffers

become increasingly complex. Such efforts are made anyway, because gate-driven amplifiers and buffers offer high input impedance and no DC current-path at input node. This property is very important in typical voltage-mode ICs, but it can be crucial in case of HV buffers playing some less ordinary roles in complex HV systems. High input-impedance buffers may build input stages of specific voltage-current converters [6], like one presented in Fig. 2. In such devices precise control over current flow is deciding for their proper operation. Any extra current flows through current/voltage conversion devices would falsify output signals of such converters. This is why buffers with input DC current paths cannot be used as output buffers of such I/V converters.

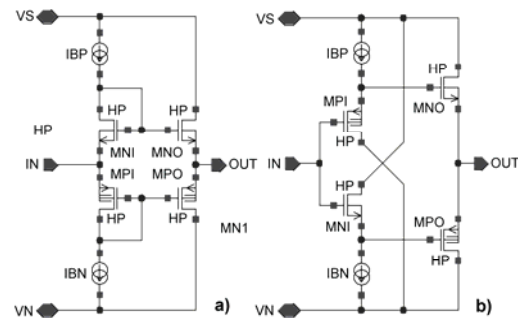


Figure 1. Typical gate-follower (a) and source-follower (b) based buffers.

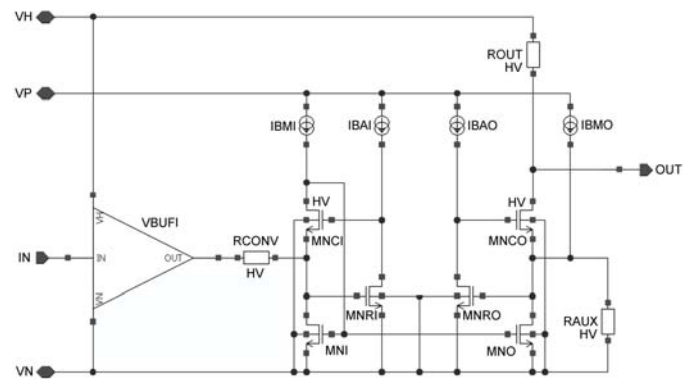


Figure 2. LV/I/HV converter – an example of circuit not well suited for cooperation with switches of Fig. 6a-b [6].

Application of gate-driven buffers amends the problem of input DC current path, but do not fully save all the current-flow problems, as fast voltage changes at buffer inputs require current-flow for parasitic capacitance recharging. Though, improvement of buffer input-stage operation quality is usually satisfactory, additional circuitry for improving inherently poorly defined operation parameters of gate-follower based

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HV buffers may deteriorate e.g. the buffer bandwidth or make it more prone to process mismatches.

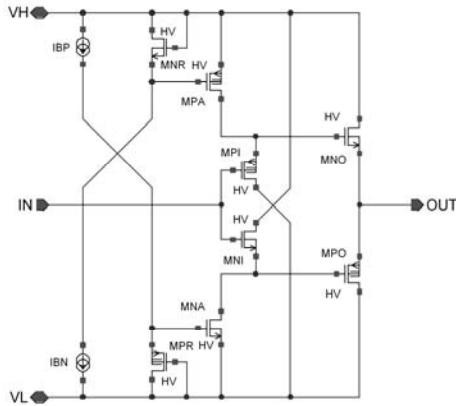


Figure 3. Simplified schematic of a gate-driven HV buffer based on both gate-follower and source-follower topologies [7].

Idea of interesting solution, proposed by the authors [7] and patented [8], is presented in Fig. 3. The main asset of the structure is that, owing to merging topologies of source-follower and gate-follower circuits, it retains best properties of both topologies – high input impedance, satisfactory voltage gain and low input-output voltage shift. Schematic presented in Fig. 3 is a simplified version with all HV MOS devices. Thus, precise operation of the circuit cannot be ensured, because of poor matching capabilities of HV transistors. Fig. 4 presents the fully functional buffer with MOS transistors most important for buffer operation implemented as LV devices buffered or shielded by HV MOS devices. Apart from more precise gain and minimized level-shift values, application of auxiliary transistors (mainly MNC and MPC) results in even higher input impedance of the proposed buffer, which is obvious asset.

What sets this topology apart from most of the proposed buffer modifications reported in literature is fact that most of the circuit modifications are placed outside its signal-path and they are DC operating devices related only to the input-stage of the buffer.

The presented structure is relatively simple, over all the signal-path remains very short. Also, the proposed topology leaves possibility of merging it with other existing derivatives of the follower-based buffers [3-5]. It is possible due to a fact that most of typical buffer modifications are placed in output-stage of the modified buffers, just opposite to the presented structure.

As HV unity-gain buffers are often based on gate-followers, source-followers and their concatenations, it is acceptable to introduce enable and power-down functionality implementations, with use of relatively simple version of complementary source-follower based unity-gain buffer.

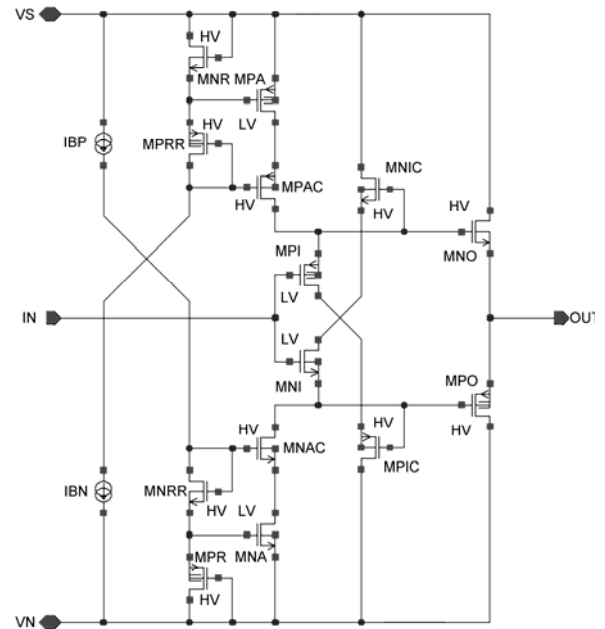


Figure 4. Gate-driven HV buffer based on both gate-follower and source-follower topologies [7].

III. CONTROL FUNCTIONALITY IMPLEMENTATION

A source-follower complementary HV buffer, based on topology presented in Fig. 1a has been selected for implementation of enable and power-down functionalities.

As it can be seen in the Fig. 5, the discussed modified buffer is equipped with two enable signal inputs – EN and PD. In order to put the buffer into power-down state, proper values of both EN and PD signals must be used. Though, the high-impedance functionality is activated with use of EN signal only. Means of control application can be changes with use of modified control-logic, of course. In the presented buffer the logic circuitry is treated as an external circuitry and thus, not included.

The PD/EN signal induced power-down mode makes all the circuit stop operating, as all bias currents are cut-off.

The EN signal present in the buffer in Fig. 5 is used for driving several aspects of high-Z functionality, both at input and output nodes.

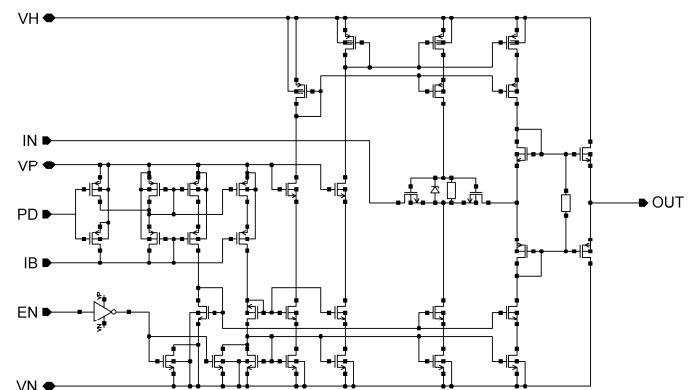


Figure 5. Modified buffer structure.

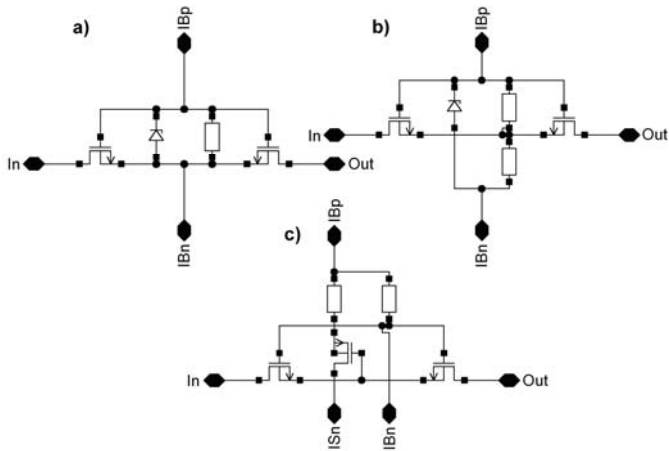


Figure 6. High-voltage current-controlled switches [9].

Of course, in practical implementations, several EN signals may be implemented, so that only selected control subcircuits are activated, while all the remaining part of buffer circuitry remains unaffected.

When the EN signal is high, the bias current mirrors feed the HV current-controlled switches with externally defined current flows. There are several structures of such current-controlled switching devices [9], some of them are shown in Fig. 6. These switches are driven each with two HV current sources. Such solution, along with resistor driven switch transistors ensures firm transition into cut-off condition for both switch transistors.

Switches presented in Fig. 6a-b do not provide complete isolation of circuit signal-path and switch control-path. As a result, these two current flows can get mixed. In case of typical voltage-mode circuits – usually it is not a problem. Though, in case of current-mode circuits complete current-path isolation is required, and other existing switch structures must be applied [9], like one presented in Fig. 6c.

The I/V converter presented in Fig. 2 is an example of a circuit which strictly requires high-impedance input of the

buffer with no DC current path, at its output node. Application of a switch, that may produce small currents sourced from or sunk into the output node of a preceding current-mode nodes, like ones in Fig. 6a-b, is a very bad idea. It could damage current-voltage conversion ratio and render the whole function block unusable.

The Fig. 6c switch is a solution in this case, too. Another example of function block that requires similar buffer structure at its output is presented in Fig. 7 [11]. This function block converts single input voltage waveform into current form and provides differential (positive and inverted) output current signal, which are converted back to voltage mode with use of single resistors same as used in V/I conversion stage.

The EN signal cuts-off HV current sources both on high and low switch sides. It can be found, that while the low-side HV current mirrors are firmly switched-off, the high-side HV current mirrors are off only because of lack of current sourced from their common input. This condition places them at the verge of conduction. But because the current flow is blocked by firmly cut-off outputs of low-side HV mirrors and both transistors of the switches, high-side induced current-flows are impossible.

Anyway, if the cut-off conditions of the high-side HV current mirrors would be considered not acceptable, there are possible remedies. First, some additional HV logic level converter might be used for providing the HV EN signal, whenever the HV ground node is present or not. Fitting logic level-shifters are presented in [10]. Moreover, a high value resistor (e.g. made of high-resistance poly2 layer, if accessible) may be applied in parallel with the input of the cascode transistor polarization circuit on the high-side of the buffer circuitry. While the input current is sourced from the above-mentioned circuit, its small fraction would be drawn from the resistor. As the current redirection results in a very limited repolarization of the cascode transistors only, all this modification is negligible for the current mirror operation quality.

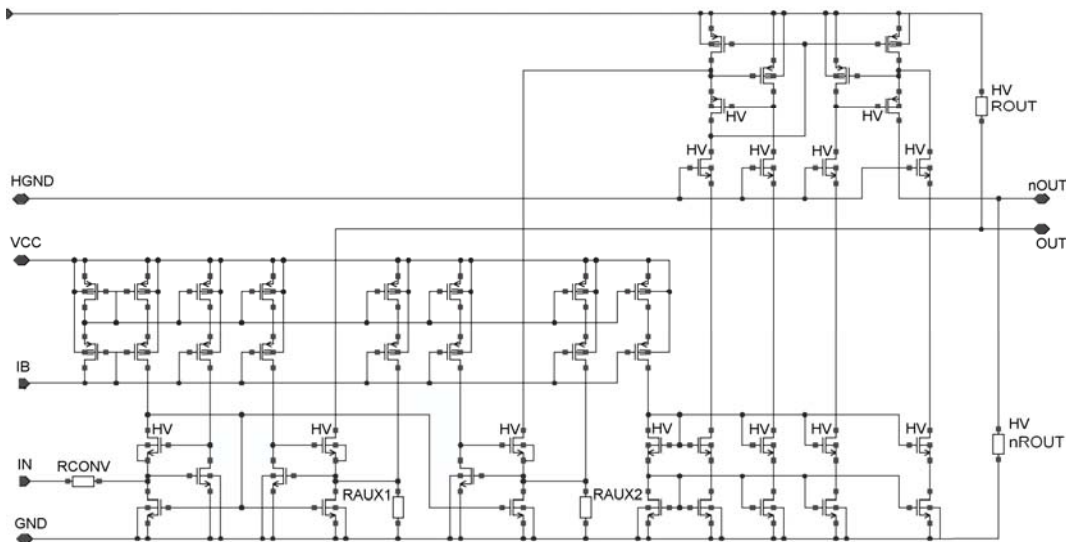


Figure 7. Function block providing positive and inverted version of input signal – an example of a circuits that requires a high input-impedance buffer.

The output side of the discussed buffer is also equipped with high-impedance functionality. When the bias currents of a typical buffer are cut-off, transistors of the buffer input- and output stage are at the verge of cut-off mode. Some large loads or load changes at the buffer output could cause the output side transistors to start conduct some amounts of current and though there still may be no input to output connection, the high-Z for the output node of the buffer is not retained.

Amendment of this problem is very efficient and straightforward – there is a resistor added in parallel to the input stage (the vertical one presented in the Fig. 5 buffer). It may be stated, that a kind of HV switch is created, but unlike the ones presented before, this one is placed vertically in voltage space. Now, the bias current of the buffer input stage is used for output stage state control, too. While the buffer bias currents are on, small amount of the bias currents flow through the vertical resistor, but due to highly non-linear current-voltage characteristics of MOS transistors used in the input stage, effect of the resistor presence can either be neglected or easily dealt with. When the bias currents cease, the resistor short-circuits gates of the input and output stage transistors of the buffer and thus keeps them firmly cut-off, as the gate-source voltage is close to 0 V.

HV current-controlled switches disconnect input of the whole buffer from the source follower structure, while the resistor-induced cut-off states of the both input and output side of the buffer cause its output to be a floating high-Z node, not related to the input voltage of the buffer.

In case the modified buffer is equipped with high-impedance input-stage, like e.g. gate-driven high-impedance input (Fig. 4), application of switches used in the buffer, as presented in Fig. 5, is not recommended. Switches with isolated current-paths must be used, instead. Switch presented in Fig. 6c is proper for this application. Unfortunately, application of such switches requires a more complicated switch-control circuitry.

Though, there is another possible approach able to provide all required high-Z functionality. This approach is possible due to presence of the high-Z input node in the original non-modified buffer. Owing to this property, the only required task for HV current-controlled switches may be separation of input- and output-stages of the buffer. In other words, the solution is to place the switches inside the complementary follower section, instead of placing them before the whole buffer. Now, the input stage of the follower isolates the HV switches from input node of the whole buffer. As a result, simple switches with non-isolated current-paths can be used with marginal influence on the buffer operation quality.

Both proposed approach ideas are presented in Fig. 8. It can be observed, that main difference between these approaches is related to fact that gate-driven buffers, like gate-followers, are equipped with high input-impedance feature and this feature only needs to be retained in the modified versions of such buffers, with on extra circuitry related to it. In case of source-follower based buffers, the high input-impedance feature is absent in the original buffers and must be provided “from scratch” in their modified versions.

It might be said, that the circuit presented in Fig. 8b is overly complicated, as two HV switches with four current sources are required in total, instead of one switch with two current mirrors, present in Fig. 8a. The internal HV switch block can be simplified by using HV switches with MOS-based I/V converters, controlled with one current source. Such circuit idea is presented in Fig. 9, along with typical buffer equipped with simple HV switch, for comparison purposes. The used switches have some problems of their own, but possible solutions are discussed in [9].

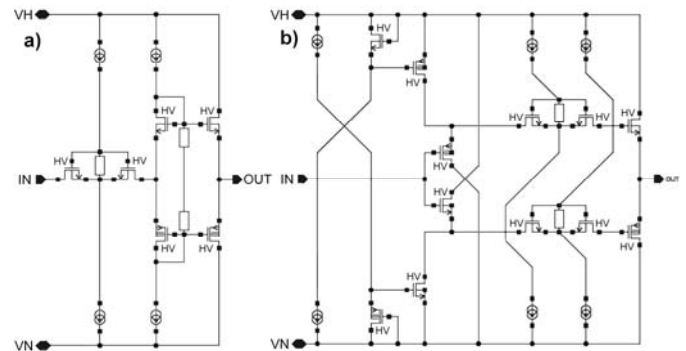


Figure 8. Application of HV switches ahead of an input buffer stage (a) and inside a buffer – between input- and output-stage of a buffer (b) [9].

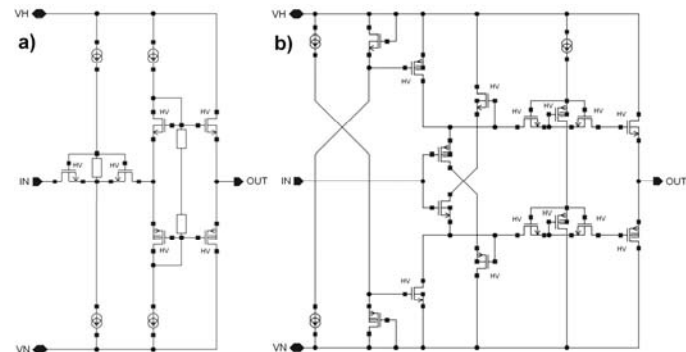


Figure 9. Application of specialized HV switches ahead of an input buffer stage (a) and inside a buffer – between input- and output-stage of a buffer (b).

IV. THE MODIFIED BUFFER OPERATION SIMULATIONS

Functionality of the modified buffer is simulated and presented for the case of source-follower based buffer presented in Fig. 5.

Fig. 10 presents the enable functionality aspect of time domain operation of the Fig. 5 presented buffer. The simulation starts for the buffer operating in normal mode, the buffer is fed with an 11 V p-p 125 kHz trapezoidal edge-rounded waveform. Next, the EN signal goes low and the output node becomes fully disconnected from the input signal. It can be observed that output signal is floating in voltage space, as the buffer output is now a high-impedance node. On EN signal going high back, the circuit starts its operation.

Fig. 11 shows voltage drop on the HV switch resistor, for high and low EN signal values. It can be seen that the resistor efficiently turns off the switch transistors and keeps them in that state. I/V conversion with use of resistive device might seem not a best approach, as it usually consumes more

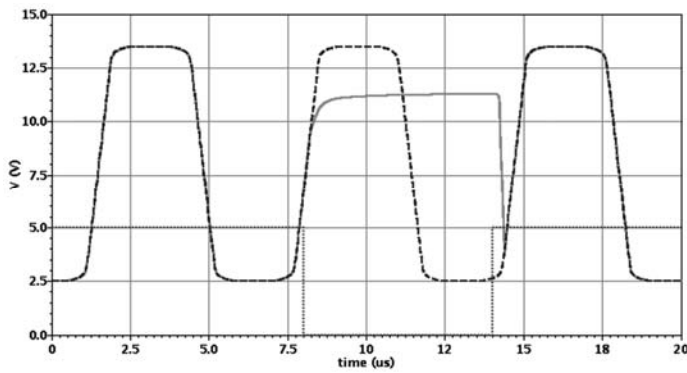


Figure 10. Buffer signals: EN - dotted, input - dashed, output – solid line.

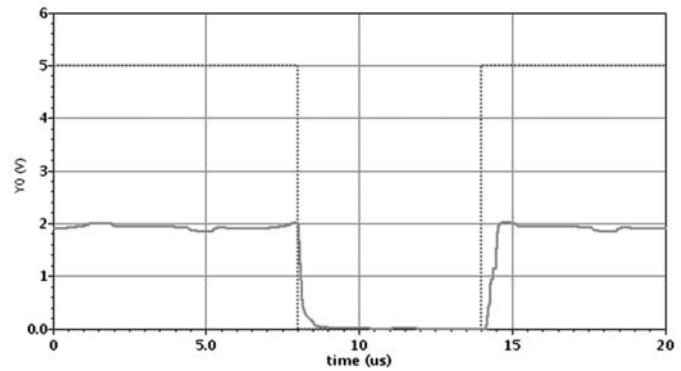


Figure 11. Operation of the buffer: signals: EN – dotted, voltage drop on the switch resistor – solid line.

semiconductor area. Though, this is a simplest sure way of forcing gate-source voltage of HV switch transistors firmly to vicinity of 0 V, so that HV MOS switch transistors can be firmly kept in off state. This would be difficult to achieve with use of MOS-based I/V converting devices.

Fig. 12 shows behavior of the buffer output stage for EN signal low and high states. The vertical resistor placed inside the buffer forces the gate-source voltages of the output-stage transistors to reach zero, while EN signal goes low and bias current-flows cease. This keeps the buffer output firmly cut-off. The simulation is performed with 1 k Ω output resistor connected to the ground node. It can be seen that the total gate-source voltage of the MOS transistors drops relatively slowly. If faster operation is required, smaller value resistor is needed. In the discussed simulation the vertical resistor value is 1 M Ω .

V. CONCLUSIONS

In the paper a set of power- and operation-control enabling modifications possible in HV unity-gain buffers, is presented. The introduced high input- and output-impedance functionality is implemented and simulated for case of a typical complementary source-follower based buffer. An alternative approach applicable for a complementary source-follower and gate-follower based unity buffers has also been presented. The proposed buffer modifications offer high impedance at input and output nodes, obtained with quite limited amount of additional auxiliary circuitry.

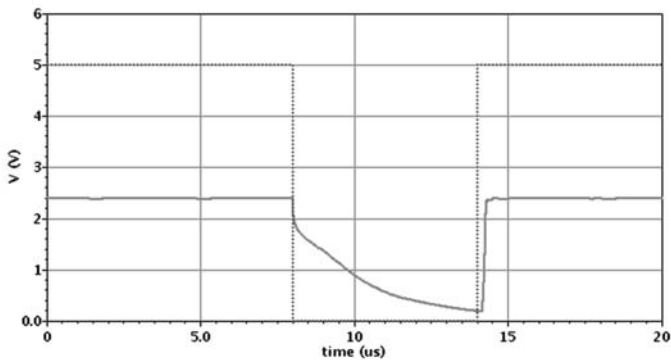


Figure 12. The buffer operation, signals: EN – dotted, total gate-source voltage on both output stage MOS transistors – solid line.

High input/output functionality build into presented buffers enables e.g. consecutive driving of several similar buffers from a single signal source, with no risk of inter-buffer disturbance transmission and with limited load imposed on the signal source node. Moreover, several such buffers may consecutively output their signals to a single next-stage input with no problem, as long as only one of such buffers is enabled to operate and total parasitic capacitance at the output node is acceptable. Thus, signal processing blocks do not need to be entirely multiplied.

The presented solutions are only a few of many possible HV current-control switch and core buffer concatenation configurations. It is worth mentioning that use of voltage buffers with no input DC current path, like based on gate-follower principle, along with internal use of simple HV switches, makes possible providing presented functionality for circuits with current-mode outputs.

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