

Heat Path Characterization from Thermal Impedance Time Domain Measurements

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Abstract—Thermal impedance measurement of semiconductor devices is one of the standard and well established methods of characterization. From such measurements can be obtained not only behavioral information in the form of graphs or models for thermal simulation, but also structural information about the thermal path involved, from source to sink, that can be very useful in device assembly process characterization and control. Structural information, however, usually requires many processing steps of measured data with its associated calculation burden and numerical errors. This work proposes a method to extract structural information from measured data in a straightforward way, with very few and elementary calculations, thus providing a useful analysis tool.

Index Terms—thermal impedance, heat path, diffusion, diffusion length, effusivity.

I. INTRODUCTION

METHODS for measuring the thermal impedance of electronic devices are well documented in literature [1-2]. For packaged devices where the active semiconductor is not directly accessible, methods are mostly based on recording the values of some suitable Temperature Sensitive Electrical Parameter (TSEP) versus time during switch-on [2-5] or switch-off [5-7] transient. Whatever the method, the final result is a series of values of the measured TSEP at measurement instants of time that constitute the thermal time response of the device.

Once the measurement is performed and data are available, several methods exist to extract both the thermal equivalent circuit and structural data. One technique [8] is based on calculating the Cauer equivalent circuit through deconvolution and network transformation and then the so called differential structure function. A second technique [9] performs a straightforward domain change from time to frequency and then calculates the Cauer equivalent circuit and the structure function. Yet other techniques to obtain structural information are based on the thermal impedance phase shift measurement in the frequency domain [10, 11].

Although the equivalent thermal model is important to characterize the behaviour of a given device and provide means for thermal or electrothermal simulation, structural

information, i.e., the association of thermal response to given parts of device physical structure is crucial to characterize the assembly process, with special mention to die attach, and thus the final device quality. The ultimate thermal performance of a packaged semiconductor device depends on the sum of numerous factors that may affect in many ways. Materials involved, from die to heatsink, as well as the way they are processed are important in the design of a good finished product, but process variations may also have a great influence. In the last category, die attach is probably the more difficult operation to hold within specified limits because it involves two interfaces (die- solder and solder-header) and a structural change of solder material during processing. Because of that, any control method that can be devised, particularly if it is easy to implement and does not imply the use of sophisticated equipment will significantly contribute to the understanding of the process and the quality of finished product accordingly. In the following paragraphs we will develop a suitable method, along with a series of experiments to state its usefulness.

II. THEORY

The thermal behavior of systems without convection and radiation is a solution of the heat conduction equation:

$$\rho c_v \frac{\partial T}{\partial t} - \text{div}(k \nabla T) = 0 \quad (1)$$

where T is the temperature, ρ the density, c_v the specific heat per unit volume and k the thermal conductivity. If we reduce equation (1) to a single dimension by considering for example the temperature value along a symmetry axis x of the structure or else some averaging process or any other simplifying assumption, and assume a constant value for the thermal conductivity we get:

$$\frac{\partial^2 T}{\partial z^2} - \frac{1}{\alpha} \frac{\partial T}{\partial t} = 0 \quad (2)$$

where $\alpha = k / \rho c_v$ is the thermal diffusivity. Any solution of equation (2) will be a function of t , x and α , i.e., time, position along the structure and material characteristics.

We remark that equation (2) is a diffusion equation so its solution can be expressed in terms of a single dimensionless variable $\xi = x / \sqrt{2\alpha t}$ [12] meaning that time and space are

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not really independent and, for a one dimensional diffusion process, the value of the diffusing quantity at a given spatial coordinate and a given instant of time is the same for the same value of $x/\sqrt{(2\alpha t)}$ ratio. This fact, inherent to any diffusion process, implies that the longer we heat the deeper the heat will reach into the structure and the larger the influence of deeper and deeper parts of the structure will have on the terminal behavior.

To clearly understand what we really do when we measure the thermal impedance, look at figure 1. On the plane $l = 0$ we apply a power step W uniformly distributed over the area A .

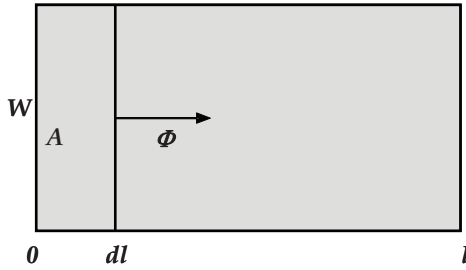


Fig. 1. Thermal Impedance definition.

The thermal impedance we see at this plane due to a slice of material of thermal conductivity k and length dl is:

$$dZ = \frac{-dT}{W} = \frac{-dT}{\Phi \cdot A} \quad (3)$$

where we put a minus sign because T decreases with l and Z has to be positive. The value of the flux is:

$$\Phi = -k \frac{dT}{dl} \quad (4)$$

If we substitute equation (4) into equation (3) we get:

$$dZ = \frac{dl}{k \cdot A} \quad (5)$$

The thermal impedance of the whole volume is:

$$Z = \int_0^l \frac{dl}{k \cdot A} \quad (6)$$

where we assume that both k and A may be functions of l . The value given in equation (6) is in fact the measured thermal impedance. Also, from equation (5) we get:

$$\frac{dZ}{dl} = \frac{1}{k \cdot A} \quad (7)$$

That contains information about the structure in the term $k \cdot A$, though we are not able to separate the material influence from k from the heat spreading implicit in A .

The performed measurement yields the value of thermal impedance versus time. However, being a diffusion process we know that in one dimensional heat conduction there is a direct relationship between time and length. We define a variable $l = \sqrt{(2\alpha t)}$ called diffusion length, that represents the time equivalent length in a material of diffusivity α . There is a substantial difficulty in doing that because the value of α is not known in advance and may change along the structure. Accordingly, the relation between time and length is not completely determined a priori.

Let's define a new variable, that we call normalized length, as $l_0 = \sqrt{(2\alpha_0 t)}$ where the dimensions of α_0 are length²/time and its value is unity. We will assume that the length unit is cm. According to this we may write:

$$\frac{dZ}{dl_0} = \frac{dZ}{dl} \cdot \frac{dl}{dl_0} = \frac{1}{k \cdot A} \cdot \sqrt{\frac{\alpha}{\alpha_0}} = \frac{1}{\sqrt{\alpha_0}} \cdot \frac{1}{b \cdot A} \quad (8)$$

where $b = \sqrt{(k\rho c_v)}$ is the effusivity of the material.

Let's analyze equation (8). If we set aside the dimensions, the derivative with respect to l_0 is equivalent, except for a factor of two, to the derivative with respect to \sqrt{t} and its value is the inverse of the product of material effusivity times the heat conduction cross section. Accordingly, because in the heat path of a semiconductor package a constriction is very unlikely, the cross section will very rarely decrease, meaning that any increase in the value of the derivative has to be attributed to a decrease in material effusivity, thus signaling an interface. Following the same reasoning other conclusions will arise in front of the experimental results.

Finally, just two remarks. First, we have assumed sharp boundaries in the calculation of thermal impedance but this is not the reality. Boundary between "hot" and "cool" volumes is diffuse and thus the spatial resolution will be limited. Second, the time to length conversion is done assuming the diffusivity value is one. This means that the length used for representation will not be the physical length and the scale will change according to the material in a way that physical length will be shorter that plot length for materials with diffusivities less than one and longer in the opposite case.

III. EXPERIMENTAL WORK

In the experimental work, the test vehicle will be a *SmartPack*[®] plastic power module, which cross section is shown in figure 2.

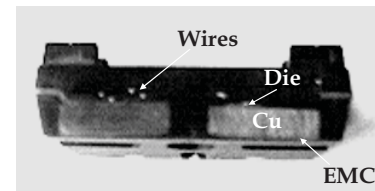


Fig. 2. Test vehicle cross section.

The package consists in a thick copper heat spreader on which the die is attached. After wire bonding the connections, the whole thing is encapsulated in a transfer moulded epoxy resin body. Relevant dimensions and material parameters are listed in table 1. In order to introduce differences in the heat path, various die attach materials and die positions will be used. A sketch is shown in figure 3 along with the two die positions used in the experiments.

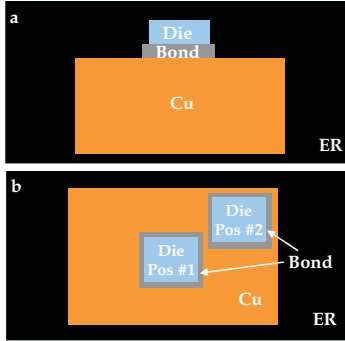


Fig. 3. Test vehicle sketch. a) Schematic cross section. b) Top view illustrating different die positions.

The test setup [8] is shown in figure 4. The Device Under Test (DUT) is connected to a controlled current power supply providing the heating current, the gate driving when required and the measuring current.

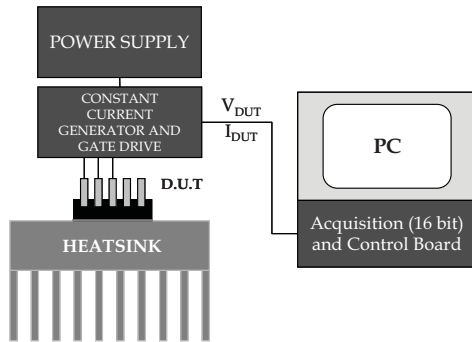


Fig. 4. Measurement set-up.

The PC application controls both the heating pulse parameters, basically duration and intensity and the acquisition of the measured quantities, i.e., DUT heating and measuring current and the TSEP voltage, through a simultaneous acquisition 16 bit AD converter capable of up to 500 Ksamples/s. The devices used in the experiments will be IGBT's, and the TSEP is the V_{CE} knee voltage at a current low enough to avoid non desired heating. Heating current will vary from 10A to 30A depending on the device and the heating time. Measuring current will be set to 50mA in most cases. Measurement of the TSEP is performed on the cooling transient and data are processed and corrected as in [6] to extend its validity up to the heating time that is set at 5s for all the runs, even if equilibrium is not achieved.

IV. MEASUREMENT RESULTS

Two sets of experiments have been performed, one using a Silver-Epoxy and a second with Sintered Silver as die attach material. Both experiments include die in positions #1 and #2 according to figure 3. Also, a former experiment using soft solder in position #1 is included. The three runs correspond to the same die (a 6.5 mm square IGBT 150 μ m thick) but different lots and different assembly runs, so some differences in results between experiments should be considered normal.

The results are presented in figure 5, that shows the thermal impedance as a function of time, and figure 6, displaying the inverse of thermal impedance derivative with respect to t_0 , i.e., the product bA of effusivity and cross sectional area. Physical constants of package materials are included in table 1.

Although the plot of thermal impedance versus time already shows, as it has to be, the difference between runs and the time scale gives an idea of where they are positioned in the structure, the plot of figure 6, displaying the product of effusivity and cross section with respect to the normalized diffusion length provides further information.

Of the three marked areas, #1 corresponds to the end of the die itself, #2 corresponds to the Ag-Epoxy die attach area and #3 marks the difference between die position #1 and #2 of figure 3.

The change in value of bA in area #2 is due to a significant decrease in the value of effusivity when going from silicon to Ag-Epoxy die attach material which is not seen in units with Sintered Ag and Soft solder because of its higher effusivity. Also, the lower thermal diffusivity value of Ag-Epoxy makes the layer to appear thicker in the figure. Its apparent thickness will in fact be about 2.5 times its physical thickness.

On the other side, the change in the value of bA product in area #3 is due to a change in heat spreading, i.e., the cross sectional area A , and happens some place going through the Cu in the corner die at position #2 of figure 3.

The first part of bA plot with positive slope is due to the electrical transient when switching the device from on to off and should be disregarded accordingly. The starting differences in area #1, the silicon, among the different devices is not clearly understood but could be due to the die itself, being from different lots, to the measurement conditions or to a not yet disclosed effect associated with die attach material and thus to temperature gradients inside the structure.

V. CONCLUSIONS

A method has been presented to extract structural information from standard thermal impedance measurements in time domain.

After running a series of experiments with different die positions and solder materials, the results show the ability of the proposed method to derive some useful conclusions concerning the package structure.

Nonetheless, more work is needed, both in measurement data processing to reduce numerical noise in differentiation and in the interpretation of some aspects of the results that may or may not be related to real phenomena.

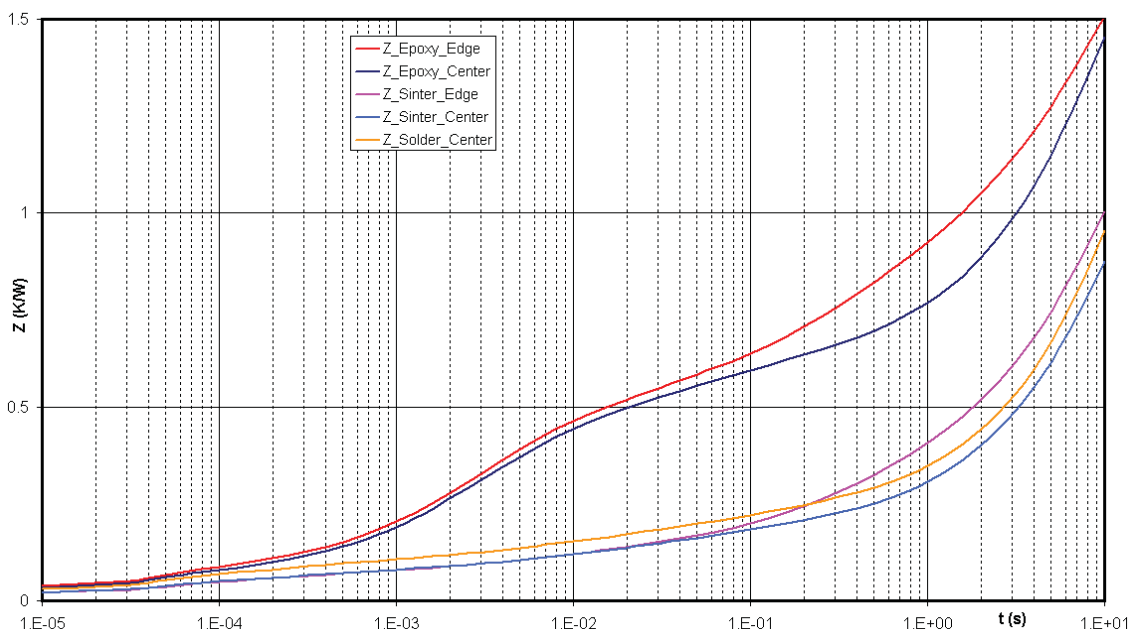


Fig. 5. Measured thermal impedance versus time.

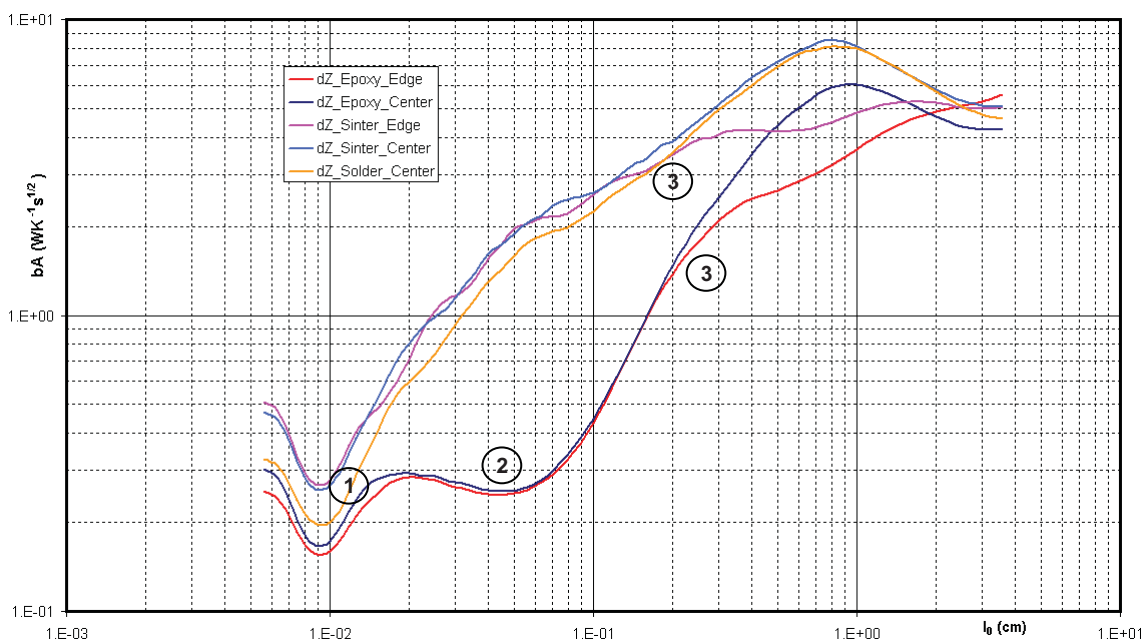


Fig. 6. Effusivity times cross section (bA) versus normalized length (l_0).

TABLE I
PHYSICAL CONSTANTS OF PACKAGE MATERIALS.

	k (Wcm ⁻¹ K ⁻¹)	ρ (gcm ⁻³)	c (Jg ⁻¹ K ⁻¹)	α (cm ² s ⁻¹)	b (JK ⁻¹ cm ⁻² s ^{-1/2})	t (cm)
<i>Si</i>	1.4	2.34	0.703	0.85	1.52	0.015 - 0.045
<i>Ag-Epoxy</i>	0.1	2.6	0.23	0.167	0.245	0.005 - 0.01
<i>Soft Solder*</i>	0.67	7.28	0.213	0.43	1.02	0.005 - 0.01
<i>Sintered Ag**</i>	2.574	7.875	0.237	1.379	2.192	0.002
<i>Cu</i>	3.4	8.96	0.35	1.08	3.265	0.4
<i>EMC</i>	0.03	2.3	1.2	0.011	0.288	0.05 - 0.07

*Data for a Tin rich solder

**Taken as a given % of bulk values. May change with sintering process

REFERENCES

- [1] "Methodology for the Thermal Measurements of Component Packages (Single Semiconductor Devices)". EIA/JEDEC Standard EIA/JESD-51. 1995.
- [2] D.L. Blackburn. "Temperature Measurements of Semiconductor Devices: A Review". Proc. SEMI-THERM 20., pp 70-80, 2004.
- [3] Z. Jacopovic. "Computer Controlled Measurement of Power MOSFET Transient Thermal Response". PESC'92 Proceedings, pp 1026-1032, 1992.
- [4] J. Zarebski, K. Gorecki. "A Method of the BJT Transient Thermal Impedance Measurement with Double Junction Calibration". 11th IEEE SEMI-THERM Symposium, pp 80-82, 1995.
- [5] Z.Jacopovic, Z.Bencic, F.Kolonic. "Important Properties of Transient Thermal Impedance for MOS-gated Power Semiconductors". ISIE'99 Proceedings, pp 574-578, 1999.
- [6] F.N. Masana. "Thermal impedance measurements under non-equilibrium conditions. How to extend its validity". Microelectronics and Reliability, Vol. 48, No. 4, pp 563-568, April 2008.
- [7] J. Zarebski, K. Gorecki: "A Method of Measuring the Transient Thermal Impedance of Monolithic Bipolar Switched Regulators". IEEE Transactions on Components and Packaging Technologies, Vol. 30, No. 4, pp:627 – 631, Dec.2007.
- [8] V. Székely, T. van Bien. "Fine structure of heat flow path in semiconductor devices: A measurement and identification method". Solid State Electronics, Vo. 31, No 9, pp 1363-1368, 1988.
- [9] F.N. Masana. "A straightforward analytical method for extraction of semiconductor device transient thermal parameters". Microelectronics and Reliability, Vol. 47, No. 12, pp 2122-2128, Dec. 2007.
- [10] K.Kurabayashi, K.E.Goodson. "Precision Measurement and Mapping of Die-Attach Thermal Resistance". IEEE Trans. on CPMT, Part A. Vol 21, No 3, pp 506-514. 1998.
- [11] F.N. Masana. "Die Attach Thermal Monitoring of IGBT Devices". MIXDES'2006 Gdynia, pp 421-424, 2006.
- [12] A.B. Kahng, S. Muddu. "Delay Analysis of VLSI Interconnections using the Diffusion Equation Model". Proc. ACM/IEEE Design Automation Conference, June 1994, pp 563-569.

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