Automated Substrate Resistance Extraction in Nanoscale VLSI by Exploiting a Geometry-based Analytical Model

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***Abstract*—In this work, a new automated method for determining the substrate resistance is presented. It exploits a geometric formulation of the current streamlines between coupled structures and builds an analytical model for the substrate resistance. Both simulation and measurement data are utilized in order to show the validity of the proposed scheme. The measurement data are obtained from a fabricated test chip. The results show that the proposed method succeeds in computing the substrate resistance while the average error falls within 5%.**

***Index Terms*—substrate noise, integrated circuits, geometric modeling, resistance extraction, resistance modeling, parasitics**

I. Introduction

THE continuous scaling of the CMOS processes has led to overall decreased distances. Additionally, future technologies like TSV [1] promise multiple device layer integration above substrate. Thus, the correct substrate noise coupling has become prominent.

Several approaches have been reported for the prediction of the noise coupling through the conductive substrate [2]-[5] yet all require the doping profile to be known. Unfortunately, this information is not disclosed by foundries. Thus, designers are trying to overcome this lack of information by other methods.

Currently, accurate doping profile determination is only possible by means of specialized techniques and instrumentation [6]-[8]. For this reason simpler techniques are necessary. In [9], the authors try to develop a rather complex methodology, which relies on a series of many different simulators, in order to avoid detailed information about doping. In [10] the resistivity is extracted by measurement data from test structures. Although, sufficiently accurate, this method requires significant amount of time and a fair knowledge of EM simulations. [11] is also based on measurement data of test structures but relies on a simulator to calibrate first an assumed doping profile and the substrate noise is computed then by a fitting model the parameters of which are extracted by the calibrated profile. Therefore it is highly dependent on the accuracy of the simulator while due to the fitting techniques employed its range of validity is expected to be limited.

In this work, a new approach for extracting the substrate resistance is proposed. It is fast, general, easy-to-use and requires a small number of simple DC measurements. Also, it does not rely on fitting techniques. The method for resistance extraction relies on the geometric interpretation and the prediction of the current streamlines between two coupled structures. The proposed scheme has been tested by utilizing data from both simulations and measurements based on a fabricated chip and also results from literature.

This work is organized as follows. In section II the formulation for the geometric substrate resistance computation is analyzed. The proposed algorithm for extracting the substrate resistance is described in section III. Simulation and measurement results are presented in section IV. The paper is concluded in section V.

II. Problem Formulation

For an accurate resistance extraction method based on measurements, an accurate and scalable formula is needed to relate the resistance of a given structure to the resistivity of the medium. Fitting techniques are not considered as an option since their range of validity is limited to certain values of their parameters. For this purpose the Substrate Resistance computation based on Geometry constraints (SRG) will be described. The SRG method is an extended version of the RCCG method [5] in order to improve the resistance extraction accuracy in epi-taxial lightly doped substrates, where the error percentage of the RCCG method is in the neighborhood of 15%, a value not adequate for an accurate resistance determination. The SRG method relies on the geometric interpretation and the prediction of the current streamlines between two coupled structures. It exploits the principle of the least energy to provide the correct geometric shape that the current flow follows. A brief description of the substrate resistance computation based on the RCCG method will be given next followed by the detailed modifications made in the SRG method in order to improve the accuracy of doping profile determination in epi-taxial lightly doped substrates.

In the RCCG method the shape approximating the current streamlines is called in general the “assumed shape”. The values that define every assumed shape and eventually the resistance itself are computed by applying the law of the least energy. Specifically, the correct shape is determined as the one which exhibits the minimum resistance. The set of

parameters that define this shape of minimum resistance are called the minimizing parameters. The resistance of this shape is the final resistance value. For the computation of the resistance of the assumed shapes, the Maxwell-Rayleigh method [12] is applied which provides an upper and a lower boundary of the actual resistance value.

The substrate resistance to the backplane of a circular contact, in particular, is given by approximating the current streamlines, Fig. 1a, with a truncated cone followed by a cylinder as shown in Fig. 1b. This approximation has been applied to both uniform and heavily doped substrates showing sufficient accuracy [5]. The final resistance value is given by the equation:

$$R_{DIP} = \frac{1}{\sigma} f(r_p, h_p) = \frac{1}{\sigma} \frac{R_{DIP}^{+} + R_{DIP}^{-}}{2} \tag{1}$$

where:

$$R_{DIP}^{-} = \frac{1}{\pi} \frac{h_p}{r_c r_p} \tag{2}$$

$$R_{DIP}^{+} = \frac{1}{\pi r_c} \frac{(r_p - r_c)^2}{h_p r_p} \frac{1}{\ln\left[1 + (r_p - r_c)^2 / h_p^2\right]} \tag{3}$$

and σ is the conductivity of the medium.

In epitaxial lightly doped substrates the truncated cone approximation breaks down. In this type of substrate, a thin layer of approximately 2 μm thickness exists above the bulk substrate having thickness of about 300 μm. The resistivity of this thin layer varies from 1 to even 1,000 times less than the bulk resistivity value. These extreme ratios of the thickness and resistivity values between the two layers lead to a very large spreading of the current streamlines in the epi-layer [13]. The assumed shapes of the RCCG method are properly modified in the SRG method to capture the above behavior with the accuracy required for doping profile extraction.

It will be detailed next, the new approach followed in the SRG method for the computation of the substrate resistance by taking into account the upper and lower boundary resistances R_m^{+} and R_m^{-}. In the computations involved, a square contact of side width w is approximated with a circular disk of the same surface area; its radius is $r_c = w/\sqrt{\pi}$. This approximation, which is followed also in [5], although not necessary for the SRG method, it greatly simplifies the involved equations.

The upper boundary resistance R_m^{+} will be determined first. The current is resolved into a horizontal (I_h) and a vertical (I_v) component, as shown in Fig. 2. The vertical current flow is approximated with a cylinder of the same cross section as the circular disk (an orthogonal parallelepiped for the square contact). The horizontal component is assumed to flow between two coaxial cylindrical shells, the first of which is the vertical one with the same cross section as the disk (two coaxial orthogonal shells for the square contact).

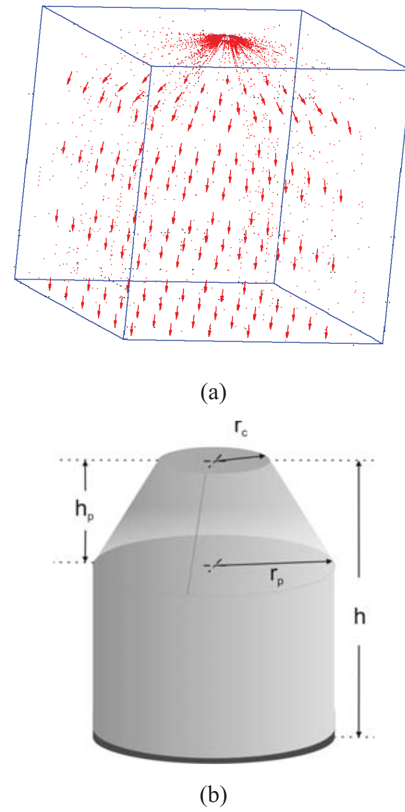

Fig. 1. Circular disk over an infinite plane (a) Electric field lines. (b) Assumed shape.

The resistance corresponding to the vertical resultant is trivial to show that it is given by:

$$R_v = \frac{1}{\sigma} \frac{h_p}{\pi r_c^2} \tag{4}$$

whereas the resistance of the horizontal resultant can be obtained by applying Gauss law, and after some calculations gives:

$$R_h = \frac{1}{\sigma} \frac{1}{2\pi h_p} \ln\left(\frac{r_c}{r_p}\right) \tag{5}$$

where the same notation as in Fig. 2 is followed.

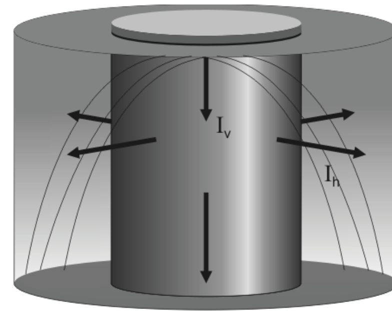

Fig. 2. Assumed current flow used in SRG method for the upper boundary resistance. A derived circular upper contact is shown at the top of the cylinder comprising the current lines.

The two resistances are assumed to be in series. Thus the final resistance value of the upper boundary is defined as:

$$R_m^+ = R_h + R_v \quad (6)$$

The lower boundary resistance R_m^- will be determined next. The equipotential surfaces are approximated as spheroid sectors parallel to the surface of the contact as shown in Fig. 3 (b). The spheroids become increasingly oblate as reaching the backplane where they become flat. The resistance between the spherical sector located at the contact and the spherical sector located at the backplane can be expressed by the definition formula of the resistance as:

$$R_s = \frac{V_1 - V_2}{I} \quad (7)$$

where V_1, V_2 is the potential at the contact and at the backplane, respectively, and I the current flowing from the first to the second. Approximating these surfaces systematically is a cumbersome task. Instead, the method of images [12] can be utilized for this purpose.

According to the method of images, the problem of a current source (CS) above a ground (or a conductive) plane can be easily solved by placing an equal and opposite CS to the symmetric position of the first CS about the plane, as shown in Fig. 3(a). The potential at any given point above the plane can be then calculated as:

$$V = \frac{I}{4\pi\sigma}\left(\frac{1}{r_1} - \frac{1}{r_2}\right) \quad (8)$$

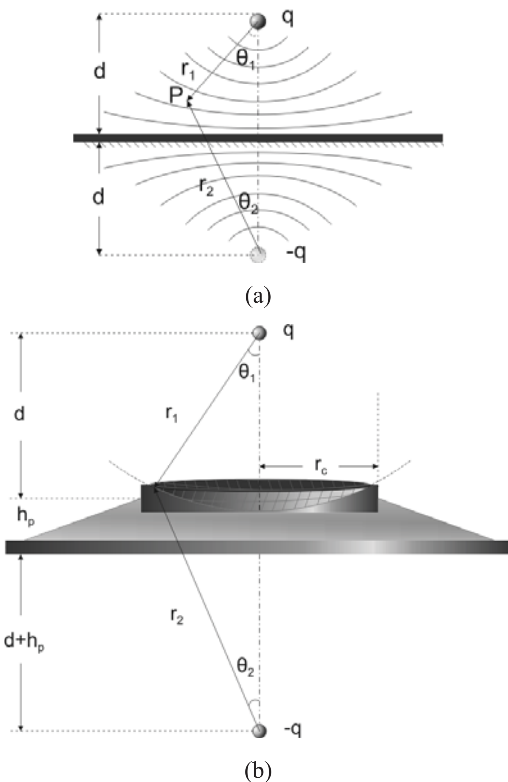

Fig. 3. Method of images a) for the charge above a perfect conductor b) applied for computing the lower boundary of the resistance.

The equipotential surfaces of this problem match that of the initial problem of the contact above a ground plane (except very close to the contact). Therefore, by substituting (8) into (7) we get for the resistance between contact and backplane:

$$R_s = \frac{1}{4\pi\sigma}\left[\left(\frac{1}{r_1} - \frac{1}{r_2}\right) - \left(\frac{1}{r_1 + h_p} - \frac{1}{r_2 - h_p}\right)\right] \quad (9)$$

Eventually, the lower boundary resistance R_m^- is computed by:

$$R_m^- = R_s / (\alpha\beta) \quad (10)$$

where the coefficients α,β are used to normalize the area of the spherical sector to that of the contact by the following way. The values of α and β are determined as follows. A CS is placed above the contact at a relatively large distance in comparison to the dimensions of the contact. This ensures that the curvature of the corresponding sphere becomes negligible in respect to the dimensions of the contact and the base circle of the spherical sector will better approximate the flat contact. The particular value used in this work is $d = 4r_c$. The spherical sector corresponds to a sphere of radius d centered at the CS having a total surface area equal to $A_{SP} = 4\pi d^2$. The surface area of the sector is $A_{SCT} = 2\pi d^2(1-\cos\theta)$. Thus, the ratio a of the latter to the area of the sphere is:

$$a = \frac{A_{SCT}}{A_{SP}} = \frac{2\pi d^2(1-\cos\theta)}{4\pi d^2} = \frac{1-\cos\theta}{2} \quad (11)$$

The surface area of the contact (circular disk) is $A_{CON} = \pi r_c^2$. So, the ratio β of the spherical sector to this area is:

$$\beta = \frac{A_{SCT}}{A_{CON}} = \frac{2\pi d^2(1-\cos\theta)}{\pi r_c^2} = \frac{2d^2(1-\cos\theta)}{r_c^2} \quad (12)$$

The final resistance of the contact to the backplane is taken, similarly to (1) as:

$$R_m = \frac{R_m^+ + R_m^-}{2} \quad (13)$$

One of the strong points of the SRG method is that it is independent of the resistivity. The latter takes the form of a simple multiplication factor to the unit resistance of the assumed shape (see equation (1) or (13)). Therefore, the calculation of the resistance of the assumed shape for each set of its parameters needs to be performed only once. Then, the resistance for every resistivity value is obtained by a simple multiplication with the unit resistance. Also, the SRG method may be directly used without any modification for the doping profile extraction of an arbitrary multi-layer substrate. As it will be shown, in section 4 the average difference of the SRG with respect to simulation and measurement results is within 5%.

III. Proposed Algorithm

The two most commonly used substrate doping profiles are the heavily doped and the lightly doped both shown in Fig.4. The substrate doping profile is not uniform in general [11].

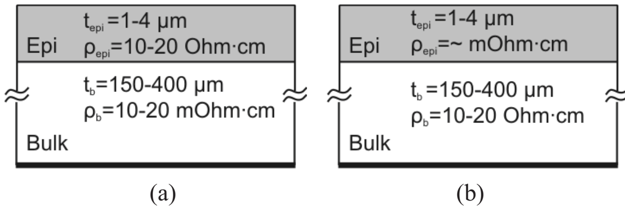

Fig. 4. Types of substrate profiles: (a) Heavily doped, (b) Lightly doped.

However the common approach, followed in this work also, is to stratify it in a number of uniform layers of specific resistivity and thickness. Every layer is then characterized by a pair of parameters at most, its thickness and its equivalent resistivity value.

The proposed method for the extraction of the substrate resistance is depicted in Fig. 5. Measurement data are first obtained by test structures on the chip under study. User introduces next in the extractor mainly the number of layers and optionally some additional parameters that will be described below. Once the resistivity has been determined the substrate coupling resistance between any two structures can be defined by employing SRG with the determined resistivity. The extractor, with the SRG approach implemented, generates a data set based on its input values which is then compared to the measurement data set. If the stop criteria, comprising mainly the relative error between the two data sets, are not met the extractor parameters are automatically refined and the procedure of generating new data set and comparing their values with the corresponding measurement data is repeated.

The measurement data used in this work correspond to the measurement of the contact to backplane resistance of each structure. There are mainly two reasons to support this choice. First, the separation of the test structures is not included as parameter to the process, which otherwise would increase the complexity of the latter (several different separation distances would be needed). The second reason is related to the area overhead due to the test structures, which is a crucial parameter for any measurement method. Here, the measurement is performed in DC implying that the structure under study is not capacitively affected by the rest of the structures in its vicinity. Therefore, the separation among them may be reduced to the smallest possible. Additionally, since the formula is independent by the dimensions of the structure, accurate characterization may be accomplished by the minimum area allowed by the process for any individual structure. Thus the area overhead, attributed to the overall area occupied by the block of test structures, can be kept very small (e.g. 0.004 mm^2 for double layer stratification).

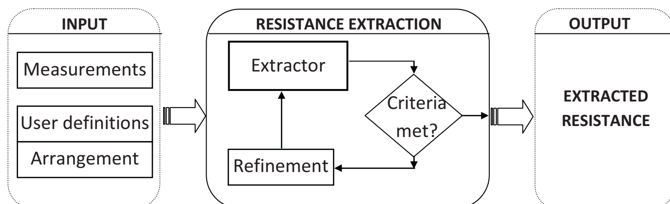

Fig. 5. Block diagram of the method for resistance extraction.

Let us consider now the extractor tool in more detail, which comprises the heart/kernel of the proposed method. The extractor takes as input the geometry of the test structures along with a set of definitions by the user and provides in each iteration a new set of resistance values. Specifically, user definitions consist primarily of the number of layers that will be used for the substrate stratification. Optionally, for each layer parameter (thickness, resistivity) specific search ranges may be defined and also an initial guess value may be given. Instead of ranges, single values may also be provided. This may be used for example to set fixed heights for each layer. Fixed values would reduce significantly the search space and consequently the overall execution time. If the initial guess value is not provided by the user, then the mean average of the upper and lower bounds of each range is used.

In the proposed resistance extraction method, two stopping criteria are employed. The first is the difference between the extracted resistance value and the measured one which should not exceed TOL value (a user defined parameter). The second one is the maximum number of iterations MAX_ITER (another user defined parameter) needed for the method to converge. After extensive experimentation, a value of MAX_ITERS=15 has been found to suffice.

IV. Experimental Results

Before applying the proposed algorithm for substrate resistivity extraction the accuracy of the SRG method is first investigated by means of a commercial simulator [14]. Finally, the proposed algorithm is validated with measurement data from a test chip.

A. Simulation Results

The computed (by the SRG method) substrate resistance value of a contact to the backplane is compared against simulation results using the FEM method as obtained from COMSOL commercial simulator [14]. First, several contact dimensions are studied for three different substrates of different resistivity and height. The results as a function of the contact dimensions are depicted in Fig. 6. As it is shown, simulation data are in close agreement with the SRG results.

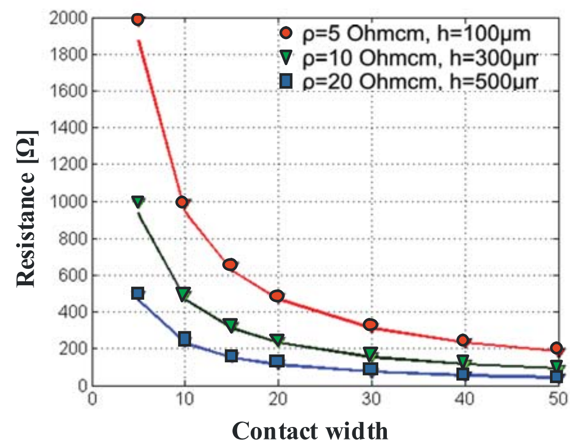

Fig. 6. Comparative results between the proposed formula and COMSOL for the substrate resistance of several contact widths and for different substrates.

Next, the SRG results are compared with COMSOL data in terms of the substrate thickness and the dimensions of the test structures for the two common substrate profiles. The dimensions of the test structures vary from 5 μm to 50 μm and the substrate thickness ranges between 100 μm and 500 μm, which cover the typical range.

The results regarding square structures are presented in Fig. 7a and b, where the relative difference between them in respect to the simulation data, is presented. Other geometries (circular, rectangular) and values have been also examined showing similar behavior. The comparison reveals, in general, that the relative difference is small, averagely about 5%. For the heavily doped substrate the biggest difference is observed for the small dimensions and falls practically below 5% for side width larger than 20 μm. For the lightly doped substrate the average relative difference is 5%.

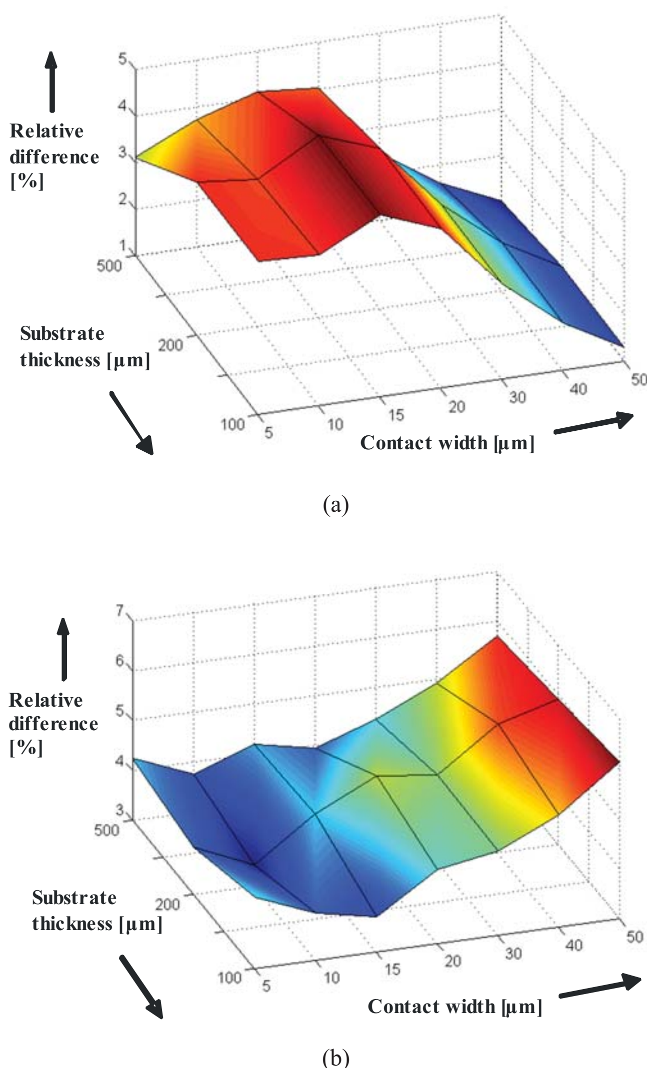

Fig. 7. Comparative results for the substrate resistance value of a contact to the backplane between SRG and COMSOL for the cases of (a) heavily doped substrate (a) and (b) lightly doped substrate.

B. Measurement Results

In this section the proposed resistance extraction method (section III) is validated against measurement data obtained by a test chip fabricated in a UMC 0.18 lightly doped CMOS process.

The resistivity of the bulk substrate is 20 Ω·cm and its height is about 500 μm. An epitaxial layer exists above the bulk substrate of about 2 μm with a resistivity ranging from a few mΩ·cm to the bulk resistivity value. The test structures consist of three arrays of square contacts of side widths 20, 30 and 40 μm as shown in Fig. 8.

The measurement setup consists of a CASCADE MICROTECH™ probe station with the probeheads [15], a HAMEG™ HM 8112-3 6 ½ digit precision multimeter [16] and the circuit under test. The probe tips attached to the probeheads are the APT™ 72T K00-17680 [17] made of tungsten and have radius 7um.

The measurements are performed in DC thus de-embedding is not needed for removing parasitics (inductive or capacitive coupling). The calibration of the multimeter is performed on the chip under test and specifically by touching a rectangular contact designed on the top metal of dimensions 25x75μm. A simple calculation reveals that for these dimensions the total resistance sensed by the probe tips would be less than 50 mΩ far less than the expected values to be measured, which vary typically above 100 Ω.

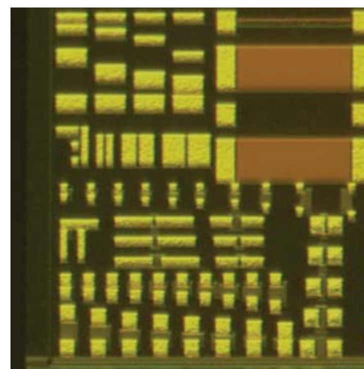

Fig. 8. Die photo of the test chip in the UMC 0.18 lightly doped process containing various contact arrangements

Table I presents the measurement results corresponding to the fabricated test chip (Fig. 8) in comparison with the results obtained by SRG. As it can be seen from the results, the prediction of the resistive coupling is in close agreement with the measurement results whereas the average error is 5.3%.

In Fig. 9, which is based on the measurement data from the fabricated test chip, the examined case involves the coupling resistance of a pair of contacts having widths $W = \{20, 30, 40\}\,\mu\text{m}$. For both cases, uniform and non-uniform, the proposed method predicts correctly the resistance coupling with the average error being approximately 5%. Also, in this figure, the proposed method has been compared against the RCCG method [5].

TABLE I
EXTRACTED RESISTANCE OF DIFFERENT TEST STRUCTURES OBTAINED BY MEASUREMENT DATA AND SRG.

Test structure w x w (μm²)	Test structure separation w (μm)	*Measurement data (Ohm)*	*SRG Data (Ohm)*	*SRG Error (%)*
20x20	5.0	268.63	278.43	3.65
	7.5	309.29	301.71	2.45
	10.0	342.41	362.03	5.73
	12.5	369.70	397.91	7.63
	15.0	393.85	384.44	2.39
	17.5	414.22	434.06	4.79
	20.0	433.62	404.65	6.68
	30.0	492.57	516.61	4.88
	40.0	535.75	555.95	3.77
30x30	5.0	187.75	197.06	4.96
	7.5	213.76	207.18	3.08
	10.0	238.90	224.09	6.20
	12.5	258.76	275.92	6.63
	15.0	277.11	260.71	5.92
	17.5	292.82	308.25	5.27
	20.0	307.00	288.92	5.89
	25.0	333.22	345.05	3.55
	30.0	353.99	374.91	5.91
	40.0	391.05	411.89	5.33
40x40	5.0	161.19	148.96	7.59
	10.0	189.02	179.61	4.98
	15.0	216.65	228.74	5.58
	20.0	237.97	221.48	6.93
	25.0	260.38	277.33	6.51
	30.0	276.19	292.82	6.02
	40.0	306.38	326.11	6.44

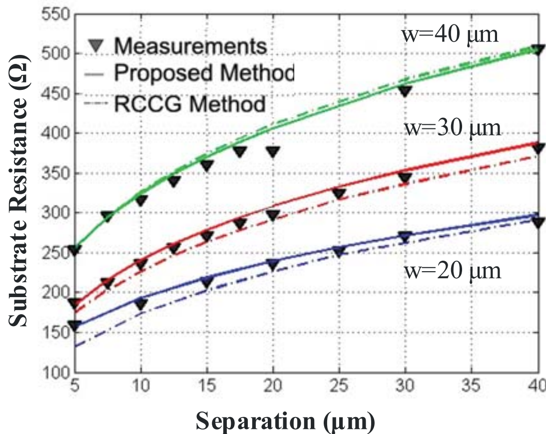

Fig. 9. Comparison of the proposed method with measurement data for the coupling resistance between two square contacts as a function of their separation. Three different side widths are studied.

V. CONCLUSIONS

An automated method for extracting the substrate resistance has been presented. It uses a geometric formulation to derive an analytical model for the substrate resistance for arbitrary substrate doping profile. The presented formulation does not rely on fitting techniques and is general. Extensive simulation experiments on various substrates heavily doped, lightly doped, and uniform have been performed. Also, measurements based on a fabricated chip have been used to validate the proposed method.

Both simulation and measurement results show that the average error in resistance computation is within 5%, supporting the validity of the proposed method.

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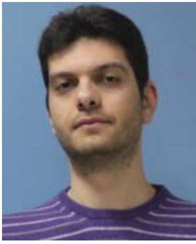

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