Analysis and Design of a MOSFET-only Wideband Balun LNA

Ivan Bastos, Luis B. Oliveira, João Goes, and Manuel Silva

***Abstract*—In this paper we present a MOSFET-only implementation of a balun LNA. This LNA is based on the combination of a common-gate and a common-source stage with cancellation of the noise of the common-gate stage. In this circuit, we replace resistors by transistors, to reduce area and cost, and to minimize the effect of process and supply variations and mismatches. In addition, we obtain a higher gain for the same voltage drop. Thus, the LNA gain is optimized and the noise figure (NF) is reduced. We derive equations for the gain, input matching and NF. The performance of this new topology is compared with that of a conventional LNA with resistors. Simulation results with a 130 nm CMOS technology show that we obtain a balun LNA with a peak gain of 20.2 dB (about 2 dB improvement), and a spot NF lower than 2.4 dB. The total power consumption is only 4.8 mW for a bandwidth higher than 6 GHz.**

***Index Terms*—CMOS LNAs, MOSFET-only circuits, Noise cancelling, Wideband LNA.**

I. Introduction

NOWADAYS, the demand for mobile and portable equipment has led to a large increase in wireless communication applications. In order to achieve full integration and low cost, modern receiver architectures (Low-IF and Zero-IF receivers), require inductorless circuits [1 - 4]. The LNA, which is a key block in the design of such receivers, is investigated in this paper.

LNAs can be either narrowband or wideband [1, 2]. Narrowband LNAs use inductors and have very low noise figure, but they occupy a large area and require a technology with RF options to have inductors with high Q. Wideband LNAs with multiple narrowband inputs have low noise, but their designs are complicated and the area and cost are high [1, 2]. RC LNAs are very simple and inherently wideband, but conventional topologies have large noise figures (NFs). Recently, wideband LNAs with noise and distortion cancelling [5] have been proposed, which can have NFs below 3 dB.

Inductorless circuits have reduced die area and cost [4]. However, they are usually realized with MiM capacitors, which require an additional insulator/metal layer, and they use poly or/and diffusion resistors, which have large process variations and mismatches.

In this paper our main goal is to design a very low area and low-cost LNA, and at the same time obtain less circuit variability, by implementing the resistors using MOS transistors (MOSFET-only design) [6]. As it will be shown, this approach adds a new degree of freedom, which can be used to maximize the LNA gain, and, therefore, minimize the circuit NF.

We start by reviewing the basic amplification stages, common-gate (CG) and common-source (CS). For each circuit we derive equations, with different levels of approximation, for the gain, input matching and noise figure. By comparing the results obtained with the different equations with those obtained by simulation, we select the level of approximation required for the frequency range in which we are interested.

For the complete LNA (combined CG and CS balun topology), we compare the conventional design with resistors, and the new MOSFET-only implementation optimized for gain and NF. Simulation results of a circuit example designed in a standard 130 nm CMOS technology validate the proposed methodology.

This paper is organized as follows. In section II we derive the equations for the basic CG and CS stages. In section III we present simulation results for the conventional LNA with resistors, which confirm the theory. In Section IV we present the MOSFET-only LNA and we describe the optimization of gain and NF. We compare performance of this LNA with others in the literature. Finally, a discussion and some conclusions are given in Section V.

II. Common-Gate and Common-Source Stages

Figs. 1 and 2 show, respectively, the CG and CS stages, normally employed in RC LNAs. We derive equations using three different levels of approximation, denoted by *a*, *b*, and *c*: *a* - transistors' complete model including the parasitic capacitances; *b* - low frequency approximation; *c* - low-frequency approximation neglecting the transistors' output resistance.

A. *Common-Gate Stage*

In the equations below g_{m1} and g_{mb1} are the transistor's transconductance and body effect transconductance, respectively, and r_{o1} is the transistor's output resistance. The capacitance C_S represents the source-bulk and source-gate

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capacitances and C_L the drain-bulk and drain-gate capacitance. R_s is the signal source resistance and R_1 is the load resistance.

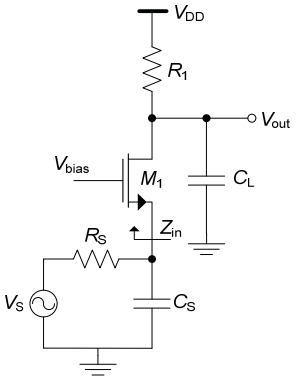

Figure 1. Common-Gate Stage.

1) Gain

$$A_{vCG\_a} = \frac{[(g_{m1}+g_{mb1})r_{o1}+1]R_1}{sC_L r_{o1}R_1+r_{o1}+R_1} \quad (1a)$$

$$A_{vCG\_b} = \frac{[(g_{m1}+g_{mb1})r_{o1}+1]R_1}{r_{o1}+R_1} \quad (1b)$$

$$A_{vCG\_c} = (g_{m1}+g_{mb1})R_1 \quad (1c)$$

2) Input Impedance

$$Z_{inCG\_a} = \frac{sC_L r_{o1}R_1+r_{o1}+R_1}{as^2+bs+c} \quad (2a)$$

where,

$$a = C_S C_L r_{o1} R_1,$$

$$b = C_S(r_{o1}+R_1) + C_L R_1(r_{o1}(g_{m1}+g_{mb1})+1),$$

$$c = r_{o1}(g_{m1}+g_{mb1})+1,$$

$$Z_{inCG\_b} = \frac{r_{o1}+R_1}{r_{o1}(g_{m1}+g_{mb1})+1} \quad (2b)$$

$$Z_{inCG\_c} = \frac{1}{g_{m1}+g_{mb1}} \quad (2c)$$

3) Noise Figure

$$F_{CG} = 1 + \frac{\gamma g_{m1}}{R_S\left(g_{m1}+g_{mb1}+\frac{1}{r_{o1}}\right)^2} + \frac{1}{R_S R_1\left(g_{m1}+g_{mb1}+\frac{1}{r_{o1}}\right)^2} + \frac{k_f}{4kTR_S c_{ox}W_1L_1 f^{\alpha f}}\left(\frac{g_{m1}}{g_{m1}+g_{mb1}+\frac{1}{r_{o1}}}\right)^2 \quad (3)$$

where k is the Boltzmann constant c_{ox} is the oxide gate capacitance *per* unit area, W_1 and L_1 are the transistor channel's width and length, respectively, T is the absolute temperature in Kelvin, γ is the excess noise factor, k_f and α_f are intrinsic process parameters, which depends on the size of the MOSFET transistors [7, 8].

B. *Common Source Stage*

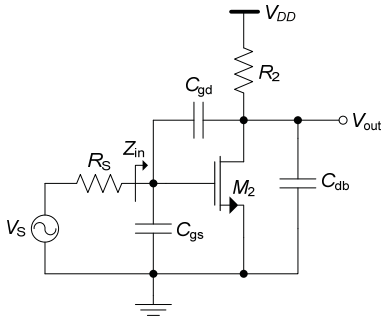

Figure 2. Common-Source Stage.

In the following equations g_{m2} and r_{o2} are the transistor's transconductance and output impedance. The capacitances C_{gs2}, C_{gd2}, and C_{db2} are the gate-source, gate-drain and drain-bulk capacitances, respectively. R_2 is the load resistor.

1) Gain

$$A_{vCS\_a} = \frac{(sC_{gd2}-g_{m2})r_{o2}R_2}{sr_{o2}R_2(C_{db2}+C_{gd2})+r_{o2}+R_2} \quad (4a)$$

$$A_{vCS\_b} = -g_{m2}\left(\frac{r_{o2}R_2}{r_{o2}+R_2}\right) \quad (4b)$$

$$A_{vCS\_c} = -g_{m2}R_2 \quad (4c)$$

2) Input Impedance

$$Z_{inCS} = \frac{r_{o2}+R_2}{s\left(C_{gs2}(r_{o2}+R_2)+C_{gd2}(r_{o2}+R_2+g_{m2}r_{o2}R_2)\right)} \quad (5)$$

3) Noise Figure

$$F_{CS} = 1 + \frac{\gamma g_{m2}}{R_S g_{m2}^2} + \frac{1}{R_S R_2 g_{m2}^2} + \frac{k_f}{4kTR_S c_{ox}W_2L_2 f^{\alpha f}} \quad (6)$$

III. LNA

In the design of a wideband LNA there is an important choice to be made. A single-ended input simplifies the connection to the antenna and RF filters (they are usually single-ended) and avoids the need of a balun for the single to differential conversion (the balun usually has high loss and degrades the NF significantly). A differential input leads to reduced harmonic distortion and to better power supply and substrate noise rejection.

In this paper we study a single-ended input LNA (Fig. 3), which combines the balun and LNA functionalities in order to obtain a simple and low cost LNA (trying to get the best of the two above described approaches).

We obtain a low noise figure LNA (NF < 3 dB), since the thermal noise of M_1 is cancelled out. The noise produced by M_1 appears in phase at the two outputs, while the signals are in opposition. Thus, we double the gain and cancel the noise. The gain matching of the two stages is critical: we need the same gain to maximize the circuit performance.

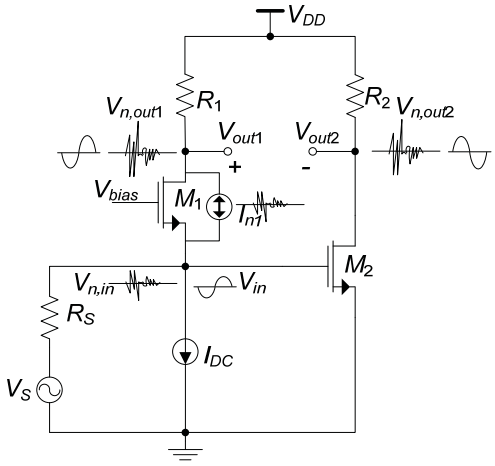

Figure 3. Balun LNA with noise canceling [9].

1) Input Impedance

The LNA input impedance is the parallel of those of the CG and CS stages,

$$Z_{inLNA} = (Z_{inCG\_a} \,//\, Z_{inCS}) \tag{7}$$

If it is assumed that the CS input impedance is very high,

$$Z_{inLNA\_a} = Z_{inCG\_a} \tag{8}$$

and if the low frequency approximation is considered (2b),

$$Z_{inLNA\_b} = Z_{inCG\_b} \tag{9}$$

2) Gain

Since the output signal is differential, and v_{out1} and v_{out2} are the CG and CS outputs, the differential gain is given by

$$A_{vLNA\_a} = A_{vCG\_a} - A_{vCS\_a} \tag{10}$$

and if the low frequencies approximations (1b) and (4b) are used,

$$A_{vLNA\_b} = A_{vCG\_b} - A_{vCS\_b} \tag{11}$$

Assuming a infinite transistor's output impedance we can simplify (11) into,

$$A_{vLNA\_c} = (g_{m1} + g_{mb1})R_1 + g_{m2}R_2 \tag{12}$$

To achieve noise cancellation and balun operation (conversion of a single-ended input to a differential output) the CG and CS's stages gain should be equal. Considering $r_{o1}(g_{mb1}+g_{m1}) >> 1$ and that for the same current and length (L) on M_1 and M_2, their output resistances (r_o) are approximately equal, and making $(g_{m1}+g_{mb1}) = g_{m2} = g_m$ and $R_1=R_2=R_D$, we obtain from (11), a fourth approximation denoted by subscript d,

$$A_{vLNA\_d} = \frac{2r_o R_D g_m}{r_o + R_D} \tag{13}$$

3) Noise Figure

Considering the approximations that lead to (13), the simplified noise figure is given by,

$$F_{LNA} = 1 + \frac{k_f}{8kTR_S g_m^2 c_{ox} f^{\alpha f}}\left(\frac{g_{m1}^2}{W_1 L_1} + \frac{g_m^2}{W_2 L_2}\right) + \frac{\gamma}{2R_S g_m} + \frac{1}{R_S R_D g_m^2} \tag{14}$$

4) Dimensions and Biasing

The LNA is designed for 50 Ω input impedance using equation (2c) as a first approximation and imposing the transconductance of M_1. M_1 is biased with 2 mA. The load resistances values are about 200 Ω to give a DC output level that avoids signal limitation and to keep M_1 and M_2 in the saturation region. The DC voltage V_{BIAS} is used to adjust the DC current of M_2 to the same value as that of M_1. The dimensions are shown on table I.

TABLE I. LNA DESIGN VALUES (CIRCUIT OF FIG. 3)

	I_D (mA)	R (Ω)	g_m (mS)	W (µm)	L (µm)	V_{BIAS} (mv)	V_{GS} (mV)
M_1	2	200	24.5	72	0.12	940	515
M_2	2	200	27.2	90	0.12	-	425

5) Simulation Results

To validate the equations obtained previously for the LNA's performance parameters, and to find out the required level of approximation, a comparison is made with the simulation results.

The real part of the input impedance (Figs. 4 and 5) remains almost constant up to 10 GHz, and the imaginary part starts to be significant above 1 GHz, so the input matching must be designed carefully for wideband applications. Equation (9) can be used for this purpose.

We confirm by simulations that equations (9) and (11) are accurate for our design, as shown in Figs. 4 to 6.

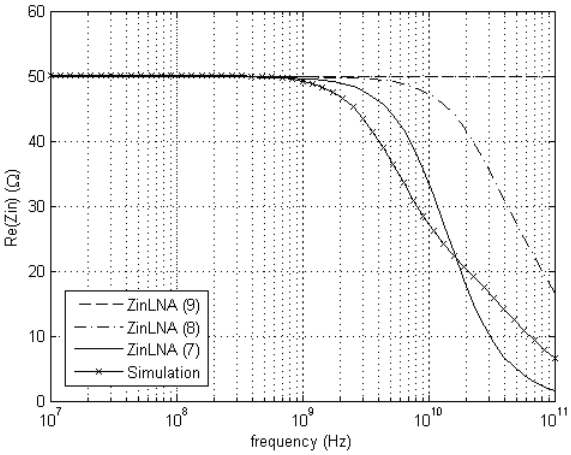

Figure 4. LNA input impedance (real part).

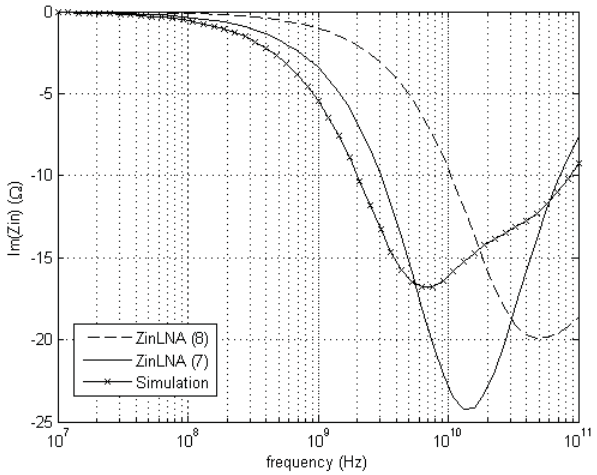

Figure 5. LNA input impedance (imaginary part).

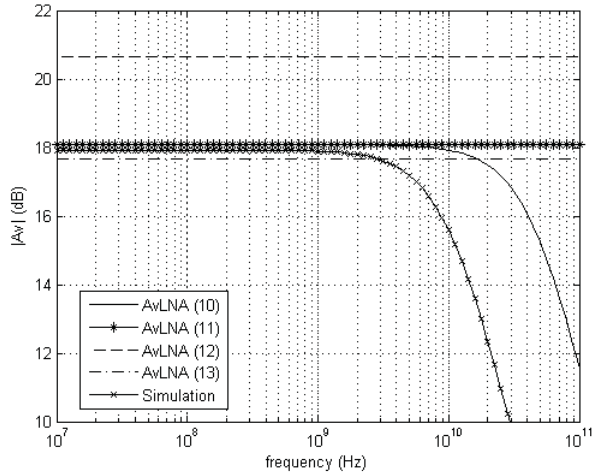

Figure 6. LNA Gain.

For the noise figure simulation we have considered $k_f = 4\text{x}10^{-23}$ V^2Hz and $\alpha_f = 1.2$ for the 130 nm technology [7,8]. We observe in Fig. 7 that the simulations are in accordance with equation (14).

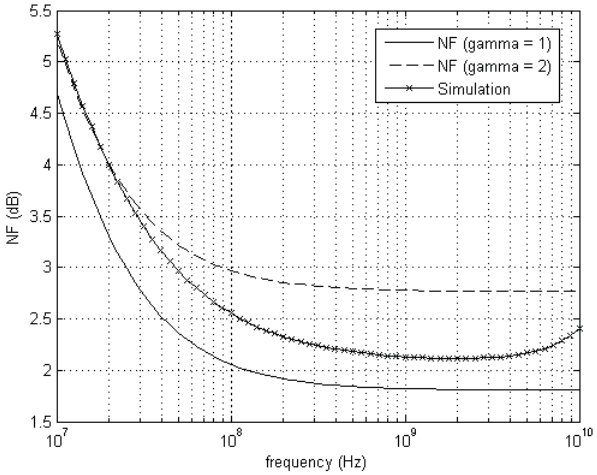

Figure 7. LNA noise figure.

IV. MOSFET-ONLY LNA

A. *Initial Design*

In the MOSFET-only LNA (Fig. 8) the load resistors are replaced by PMOS transistors (M_3, M_4) operating in the triode region, which are modeled ideally by a resistor between the drain and source,

$$(r_{ds} = 1/g_{ds}) \tag{15}$$

where g_{ds} is the channel conductance. To make a comparison with the LNA with load resistors, in the initial design, r_{ds} is dimensioned to have the same resistance value of 200 Ω. The biasing parameters are shown in table II.

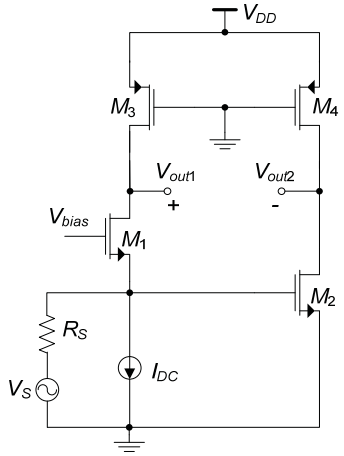

Figure 8. MOSFET-Only LNA

TABLE II. MOSFET-ONLY DESIGN VALUES (INITIAL DESIGN)

	I_D (mA)	r_{ds} (Ω)	g_m (mS)	W (µm)	L (µm)	V_{BIAS} (mv)	V_{GS} (mV)
M_1	2	-	25.38	75.6	0.12	935	507
M_2	2	-	26.73	82.8	0.12	-	427
M_3	2	206.2	2.06	15.3	0.12	-	-
M_4	2	208.3	2.09	15.3	0.12	-	-

However, once the resistors are replaced by MOSFETs, it becomes possible to optimize the initial design, as explained in the following.

B. *Optimization Results*

The saturation region is reached when g_m is of about the same magnitude as g_{ds}. A MOS transistor operating in triode region can be modeled by a resistor if $g_{ds} / g_m > 10$, otherwise the transistor should be modeled by a resistance in parallel with a current source. In this case we can increase the incremental load resistance without increasing the DC voltage drop. This allows the gain to be increased with respect to the circuit with true resistors. By simulations we find the boundary between triode and saturation (Fig. 9) and we obtain the gains and the NF as a function of g_{ds} (Fig. 10).

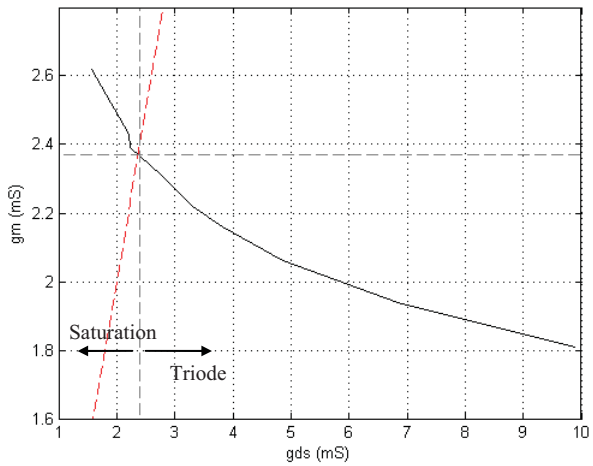

Figure 9. Transistor g_m (g_{ds}) curve.

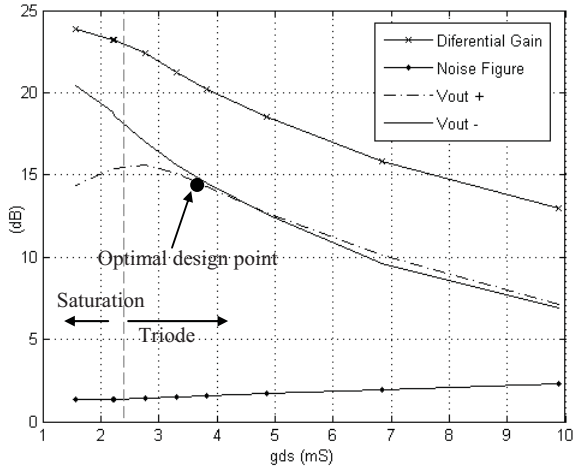

Figure 10. LNA gain optimization.

By inspection of Fig. 10 we find that the optimum operation is just before the gain of the two stages becomes unbalanced ($g_{ds} \approx 3.8$ mS), which occurs before the load transistors reach saturation. The circuit parameters are given in table III.

TABLE III. MOSFET-ONLY DESIGN VALUES (OPTIMIZED)

	I_D (mA)	r_{ds} (Ω)	g_m (mS)	W (µm)	L (µm)	V_{bias} (mv)	V_{GS} (mV)
M_1	2	-	25.23	75.6	0.12	945	513
M_2	2	-	26.74	82.8	0.12	-	432
M_3	2	261.8	2.16	13.5	0.12	-	-
M_4	2	266	2.2	13.5	0.12	-	-

C. *Simulation Results*

1) Pre-Layout Simulation

In Figs. 11-13, we present the simulation results for our MOSFET-only design (initial and optimized) and we compare them with the traditional LNA with resistors.

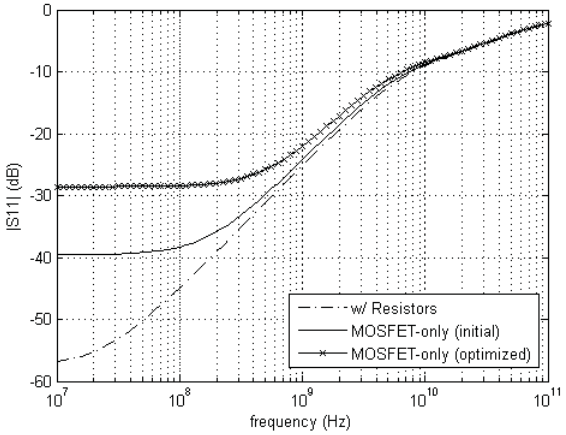

Figure 11. LNA input impedance.

The LNA is considered input matched for values below -10 dB for $|S_{11}|$, which is achieved in a band of about 8 GHz for these designs (Fig. 11)

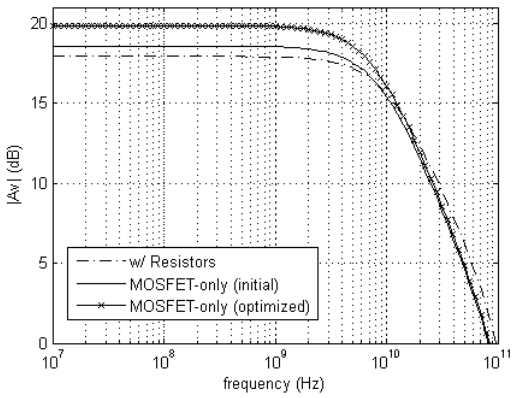

Figure 12. LNA Gain.

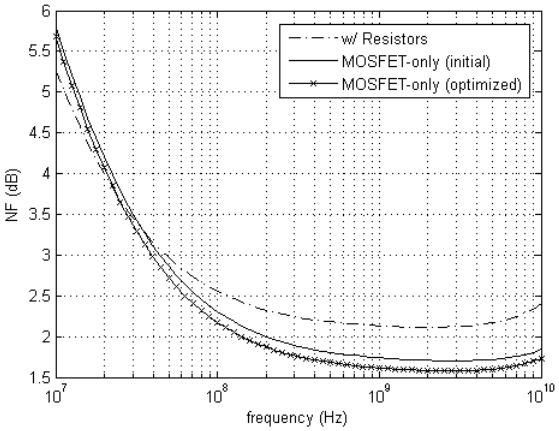

Figure 13. LNA Noise Figure.

The MOSFET-only LNA with optimized gain has an improvement of 2 dB over the traditional design, but has less bandwidth. Considering the NF, we obtain less than 2 dB from 200 MHz to 10 GHz (0.5 dB reduction) for the MOSFET-only implementation.

2) Layout design and Post-Layout Simulations

The proposed MOSFET-only LNA layout is shown in Fig. 14, has a die area of 31 x 30.5 μm². For the layout implementation, the MOSFET sizes are adjusted to minimize the poly gate resistance, and V_{bias} is tuned to set the same current for M_2 and M_4.

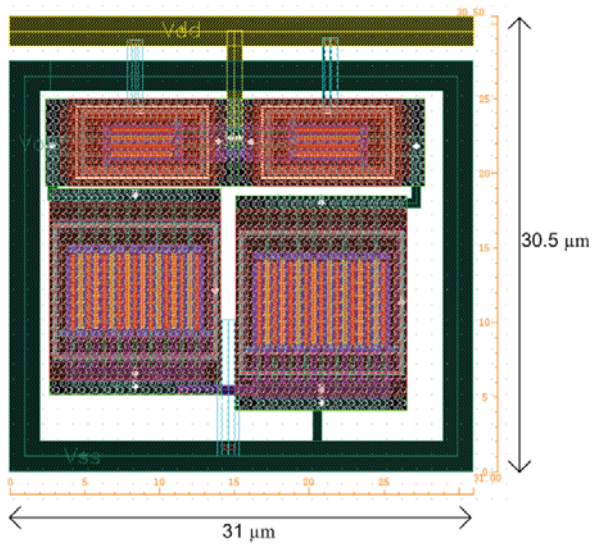

Figure 14. MOSFET-Only LNA layout.

The final layout design parameters are listed in table IV.

TABLE IV. POST-LAYOUT VALUES

	I_D (mA)	r_{ds} (Ω)	g_m (mS)	W (μm)	L (μm)	V_{bias} (mv)	V_{GS} (mV)
M_1	2	-	25.5	80	0.12	925	503
M_2	2	-	27.1	89.6	0.12	-	422
M_3	2	252.4	2.1	12.3	0.12	-	-
M_4	2	252.2	2.1	12.3	0.12	-	-

The post-layout simulation results for the main LNA parameters are shown in Figs. 15-17.

The post-layout simulations show that the input matching is not affected (Fig. 15): in fact there is a slight improvement, since the equivalent resistance of the load transistors is closer to the initial design value.

The gain increases, since the tranconductances of M_1 and M_2 increase, and, consequently, the bandwidth decreases (Fig. 16).

The main difference relatively to the pre-layout results is in the NF, which increases by approximately 0.5 dB. This is due to the thermal noise of M_1 not being fully cancelled out beyond 1 GHz. This is shown by the frequency response from the M_1 noise source to the outputs of the two stages, shown in Figs. 18 and 19 (the thermal noise due to M1 at the outputs should be equal and have the same phase for full cancellation).

If we adjust the layout to obtain full cancellation, there will be mismatches in the gain and DC offsets and, thus, the LNA becomes unbalanced.

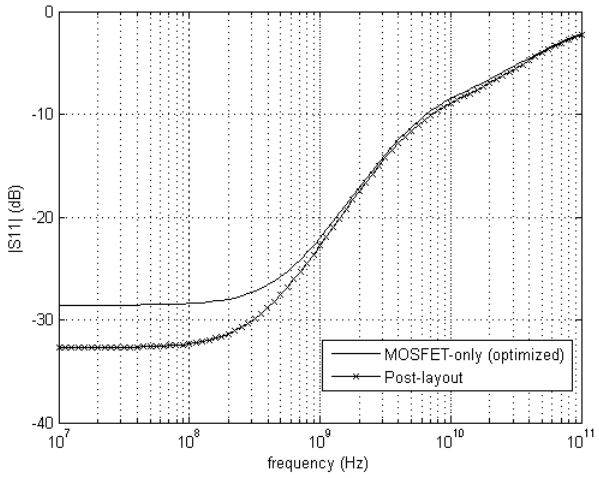

Figure 15. Input impedance.

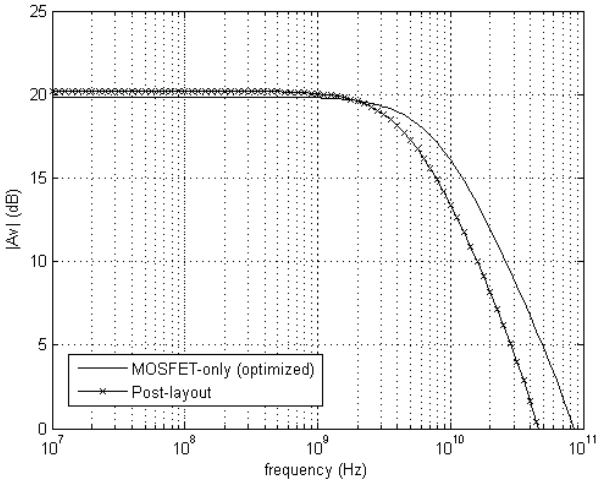

Figure 16. Gain.

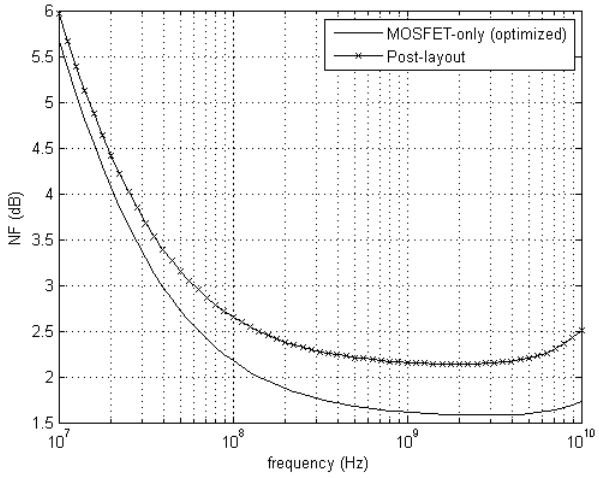

Figure 17. Noise Figure.

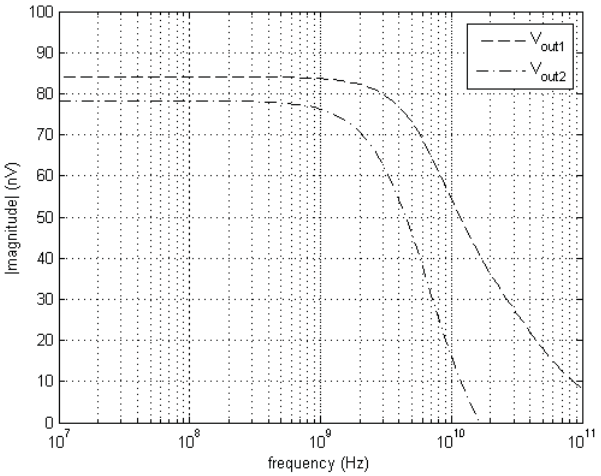

Figure 18. Noise transfer from M_1 to the outputs of the two stages (magnitude).

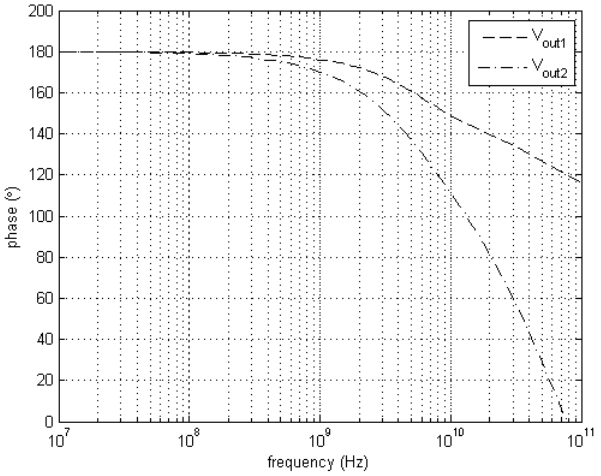

Figure 19. Noise transfer from M_1 to the outputs of the two stages (phase).

Comparing the results of our optimized MOSFET-only design with those for alternative state-of-the-art inductorless LNAs (Table V), we can conclude it has the advantages of higher gain and lower NF; the drawbacks are a reduction of bandwidth and the increase of the circuit non-linearity (reduction of IIP3).

TABLE V. LNA COMPARISON

	Tech. (nm)	Band (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Balun
[9]	65	0.2-5.2	13-15.6	< 3.5	>0	14	YES
[10]	90	0.5-8.2	22-25	< 2.6	-4/-16	42	NO
[11]	90	0.8-6	18-20	< 3.5	>-3.5	12.5	YES
[12] (sim)	90	0.1-1.9	20.6	< 2.7	10.8	9.6	YES
[13] (sim)	130	0.2-3.8	11.2	< 2.8	-2.7	1.9	YES
This work MOS	**130**	**0.2-5.1**	**20.2**	**<2.4**	**3.1**	**4.8**	**YES**

V. DISCUSSION AND CONCLUSIONS

In this paper we present a MOSFET-only implementation of an LNA based on the combination of a common-gate and a common-source stage. We derive simple equations for gain, input matching, and noise figure, which are validated by simulation.

In MOSFET-only LNAs, the replacement of resistors by transistors reduces the area and cost and minimizes the effect of process and supply variation and of mismatches [6]. Moreover, the LNA gain can be controlled by changing the bias of the PMOS transistors that replace the resistors.

The new approach proposed here adds a new degree of freedom, which can be used to optimize the LNA gain and minimize the noise figure: we can obtain a higher gain than with resistors for the same DC voltage drop. As a drawback, this approach increases the distortion (decrease of IIP3).

Simulation results of a circuit implemented in a 130 nm CMOS technology are presented. For comparison, we also show the performance of a conventional LNA with resistors. Both circuits have the same power consumption of 4.8 mW. For the MOSFET-only LNA we obtain a gain improvement of 2 dB, and a NF below 2.4 dB.

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