A Solution to Low Power Switched Capacitor Integrator Design with Reduced Effective Input Capacitance

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***Abstract*—A novel low power Switched Capacitor Integrator with reduced effective input capacitance is proposed in this paper. It is mainly based on reducing the effective input sampling capacitance by charge sharing with an extra capacitance, such that the integration capacitance can be chosen much smaller while maintaining the same sampling to integration capacitance ratio. Reducing the integration capacitance will result in less integration current and less integration current will in turn result in less power over the integrator which is the main goal of this work, reducing the integrator power consumption and chip area. Another main advantage of this configuration is, that it can be used in large time constant integrators without using physically large integration capacitance.**

***Index Terms*—Low power integrator, very large time constant integrator, effective capacitance reduction, switched capacitor integrator.**

I. Introduction

SWITCHED Capacitors (SC) are used as resistors, since they have better accuracy and they consume less die area than other resistor implementations in integrated circuits. In this technique, a capacitor is charged and discharged in order to transfer charge. This charge transfer is related to applied voltage and the value of the capacitance. Transferring charge from one node to the other one with switching gives the ability to control the charge transfer rate in a given time which means controlling the current. Changing the current between two nodes means changing the resistance between these two nodes. The value of this capacitance determines the total charge transferred in one switching cycle and the frequency of repeating this charging and discharging determines total charge transferred from one node to the other node.

Integrators are mainly formed with a resistor, a capacitor and an opamp. In switched capacitor integrators, the resistor is replaced by the switched capacitor counterpart. Output signal of the integrator is related with input frequency, switched capacitor sampling frequency, sampling capacitance and integration capacitance.

In high frequency applications charging and discharging of a capacitor becomes very important. Switching transistors must be enlarged to reduce the resistance of the switch for proper charging and discharging. However, increasing the switching transistor sizes causes an increase in the charge injection, clock feed-through and parasitic charge sharing error and in general, parasitic charge sharing is less compared to other two effects.

Another important design issue is choosing the capacitance values. Its desirable to choose as small as possible capacitance for power consumption and chip area consideration, however, capacitance sizes can not be shrunk too much because of the parasitic effects of charge injection and clock feed-through error. To minimize the charge injection and clock feed-through error, several configurations are used [1],[2],[3],[4],[5],[6].

Choosing the sampling capacitance size becomes very important at SC integrators for two main reasons. First, if the sampling capacitance size is increased, it cause to store more charge on sampling capacitance and injected charge will be less effective meaning that, error related to charge injection and clock feed-through will be less. However, there could be timing violations for proper charging and discharging especially at high frequencies and also it will increase the power consumption of the whole integrator (which will be examined in more detail at next sections) and it will consume much chip area. Second, if the sampling capacitance size is decreased, injected charge over stored charge ratio gets bigger which will result increasing the error. Also, if the sampling capacitance size is decreased, parasitic effects related to connection lines will increase the error in addition to the charge injection and clock feed-through error.

To observe the relation between the sampling capacitance size and the charge injection and clock feed-through error, two conventional switched capacitor integrators are built; one has 0.1 pF sampling capacitance and the other one has 1pF sampling capacitance and both having 6 μm width and 0.4 μm length of transistors as switches. 100 mV is applied as input signal to both circuits. Both circuits are built with TSMC 0.35 μm CMOS transistors in Cadence environment and simulated with spectre. The voltages of the two circuits sampling capacitances can be seen in Figure 1. The applied two non-overlapping clock signals can be seen in Figure 1. The clock signal which started almost at 25.05 μs and stopped at 25.4 μs is the charging clock signal and the signal which started almost at 25.55 μs is the discharging clock signal, and between these two signals, charge injection and clock feed-through errors takes place. The output signal which is marked with 100.173 mV belongs to 0.1 pF sampling capacitance circuit and the output signal which is marked with 100.003 mV belongs to 1 pF sampling capacitance circuit.

Error at 0.1 pF sampling capacitance is:

100.173-99.976=0.197 mV and

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Error at 1 pF sampling capacitance is:

100.003-99.976=0.027 mV

It can be seen from the simulation results that error of 0.1 pF sampling capacitance is 7.3 times of 1 pF sampling capacitance ones but not ten times as expected from the sampling capacitances ratio. It can be related to other parasitic effects such as parasitic charge sharing between sampling capacitance and parasitic capacitances of transistors. In real IC design; however, there will be added extra parasitic capacitances from connection paths and extra errors related to mismatching which can increase or decrease this error ratio.

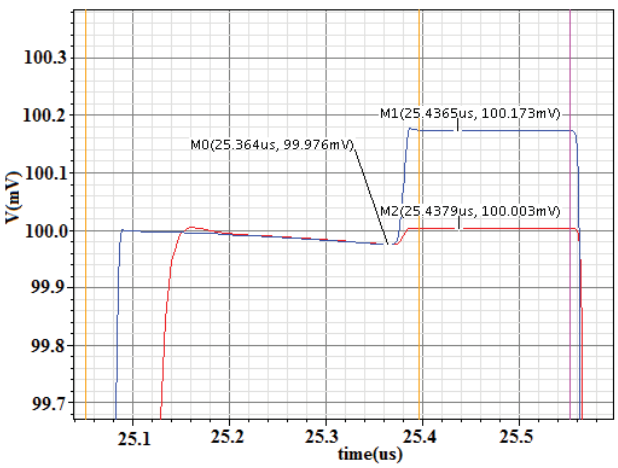

Fig. 1. Error comparison of sampling capacitances of 0.1 pF and 1 pF

To sum up, there is a trade-off for choosing the sampling capacitance size for error versus power consumption and chip area. With effective input capacitance reduction, sampling capacitance size can be increased without actually increasing the total integrators power consumption and chip area. Thus, with this architecture a low power integrator which also has less charge injection and clock feed-though error can be builded.

From power consumption point of view; the main power consumption of the integrator comes from the opamp. Thus, to make a less power consuming integrator, opamp power consumption must be decreased. However, at high frequencies, opamps power can not be reduced too much because of the high demand of the integration current. With this novel reduced effective input capacitance switched capacitor integrator architecture, integration current can be reduced without any performance degradation. In this architecture an equivalent sampling capacitance is obtained which is very small compared to its original value. With this reduced sampling capacitance, integration current is reduced drastically. To maintain the same sampling to integration capacitance ratio, integration capacitance can be made smaller. Also, reducing the integration capacitance will reduce the slew rate demand of the opamp, thus decreasing the power consumption of the opamp. Hence, with this new architecture low power integrators can be achieved.

Another feature of the reduced effective input capacitance SC integrator is, that it can be used in large time constant integrators. Large time constant integrators need large sampling to integration capacitance ratio. For less error, sampling capacitance can not be chosen too small; thus, to obtain a large capacitance ratio, integration capacitance must be enlarged. Increasing the integration capacitance results in more power to drive this big integration capacitance and also consumes large chip area. With reduced effective input capacitance switched capacitor architecture, effective sampling capacitance can be reduced which will result in decreasing of the integration capacitance with maintaining the same capacitance ratio. In this way, integration capacitance is reduced physically with the same capacitance ratio, thus if needed, integration capacitance can be increased to its maximum allowable value to obtain a very large capacitance ratio. For large time constant integrators, various architectures [7],[8],[9],[10],[11] are used to maintain the same capacitance ratio without actually increasing the integration capacitance.

This paper is organized into seven sections. Conventional SC integrators output is formed and calculated in section II. Basic working principle of the reduced effective input capacitance SC integrator and offset of the integrator is explained in section III. Low power consumption consideration is examined in section IV. Comparison of conventional and reduced effective input capacitance SC integrator is indicated at section V. Simulation results and comparisons are indicated in section VI. Finally Conclusions are drawn in section VII.

II. Conventional Switched Capacitor Integrator

In this section, conventional SC integrator will be analyzed. First switched capacitor resistor equivalent value will be substituted into the integration equation. Taking C_s as the sampling capacitor, f_s as the sampling frequency, f as the input frequency and V_{in} as the applied input signal, output is calculated. Considering the input signal as a sinusoidal wave, the output is:

$$V_{out}(\mathrm{t}) = \frac{C_s.f_s}{C_{\mathrm{int}}} \int V_{in} \sin 2\pi f t.dt = A + \frac{-V_{in}.C_s.f_s.\cos 2\pi f t}{C_{\mathrm{int}}.2\pi f} \tag{1}$$

$$Output\ amplitude:\ V_{out} = A + \frac{-V_{in}.C_s.f_s}{C_{\mathrm{int}}.2\pi f} \tag{2}$$

III. Basic Working Principle

The detailed working principle of this architecture will be examined in each clock phase in this section. In the first clock phase Q_1, the main sampling capacitance is charged with the source signal and its output voltage is the same as the input signal at the last moment of the phase Q_1. At the second phase Q_2, C_s which is the main sampling capacitance and C_{shr} which is the charge sharing capacitance are connected in parallel and the charge at C_s passes to C_{shr} until their voltages are equal to V_{shr}. Choosing charge sharing capacitance C_{shr} much bigger than the main sampling capacitance C_s, the remaining charge at C_s will be very little compared to its initial charge after Q_1 phase. At the Q_3 phase, charge which is left at C_s from the Q_2 phase will be sent to the integration

capacitance for completing the integration process. However, charge remaining at C_{shr} after the Q_2 phase, must be reset to zero initial value for the next charge sharing process. It is done at the Q_1 phase before the charge sharing occurs. This charge cleaning can be done at the Q_3 phase; however, if it is done at the Q_3 phase, it can be charged by the leakage current during the Q_1 phase and stored charge on C_{shr} will cause errors; for this reason, charge cleaning must be done at the Q_1 phase before charge sharing event happens at phase Q_2. Conceptual implementation of reduced effective input capacitance switched capacitor integrator can be seen in Figure 2 and actual circuits reduced effective input capacitance input part can be seen in Figure 3. Two right arrows show output of this part, which goes to the integrator. Fully differential class AB based integrator can be seen in Figure 4, right arrows show input signals coming from SC input part. Conventional switched capacitor integrator input part can be seen in Figure 5 and integrator part is the same which is shown in Figure 4.

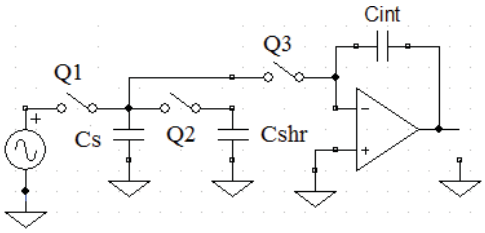

Fig. 2. Conceptual implementation of reduced effective input capacitance SC Integrator

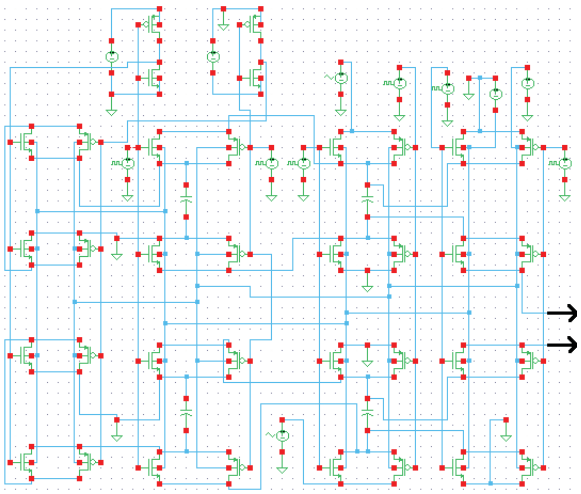

Fig. 3. Reduced effective input capacitance Switched Capacitor input part

Effective sampling capacitance perceived by the integrator can be found with:

$$V_{in}.C_s = Q_s \tag{3}$$

$$Q_{shr}(t=0) + Q_s = 0 + Q_s = Q_s \tag{4}$$

$$V_{in}.C_s = (C_s + C_{shr})V_{shr} \quad \Rightarrow \quad V_{shr} = \frac{V_{in}.C_s}{C_s + C_{shr}} \tag{5}$$

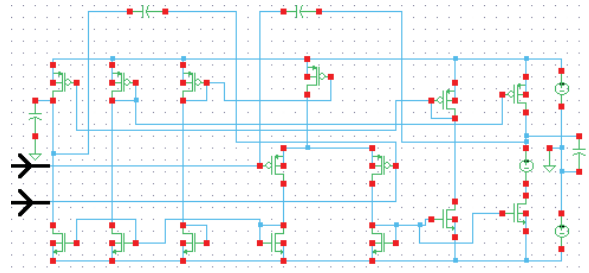

Fig. 4. Fully differential Class AB integrator part

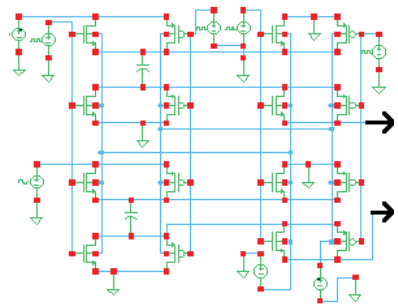

Fig. 5. Conventional Switched Capacitor integrator input part

$$Q_{Cs} = C_s.(\frac{V_{in}.C_s}{C_s + C_{shr}}) \qquad \mathrm{C}_{s\_equ} = \frac{Q_{Cs}}{V_{in}} \tag{6}$$

$$Equivalent \quad C_s \ is: \ C_{s\_equ} = C_s(\frac{C_s}{C_s + C_{shr}}) \tag{7}$$

Reduced effective input capacitance SC Integrator output signal amplitude can be calculated from (2) and (7), as:

$$V_{out}(\mathrm{t}) = A \ + \ \frac{-V_{in}.{C_s}^2.f_s}{(C_s + C_{shr}).C_{\mathrm{int}}.2\pi f} \tag{8}$$

A. Integrator Offset

Taking integral of a signal causes a DC temporary offset in addition to the main integrated signal. This DC offset settles to zero after some time depending on the amount of charge stored on the integration capacitance and the resistive load. To bring out the effects of the DC offset settling behavior and other possible secondary effects, fully differential Class AB output opamp is used rather than a CMFB opamp configuration in simulations.

Simple integration of sine is cosine and cosine starts at 1 does not start at 0 mathematically, however, at integrator output does not start abruptly at 1. Initially starting at zero voltage causes an offset voltage at the integration capacitance which will result in accumulated charge on the integration capacitance. This offset charge dissipates at the output load and self load of the output stage and this offset settles to zero DC value after some time. This offset can be explained with the integral of a sine function.

$$V_{out}(t) = \int V_m \sin 2\pi f t.dt = A - V_m \cos 2\pi f t \,{}_0^T \tag{9}$$

with boundary condition at $t = 0$ and $V_{out} = 0$

$$A - V_m \cos 2\pi f t \,{}_0^T = 0(t=0) \tag{10}$$

$$A - V_m \cos(0) = 0 \quad \Rightarrow \quad A = V_m \tag{11}$$

$$V_{out}(t) = V_m - V_m \cos 2\pi f t \tag{12}$$

Charge stored with V_m at the C_{int} is:

$$Q_{offset} = C_{\text{int}}.V_m \tag{13}$$

This temporary DC offset charge is unwanted, because offset voltage of the output changes during dissipating this extra charge and DC offset voltage caused by this temporary charge is generally compensated by the Common Mode Feedback circuit. During this settling process, output voltages are adjusted by the CMFB circuit by taking two outputs of integration capacitance. Thus, for the adjustment of this offset voltage difference between the offset voltage of the integration capacitance and the voltage of the output stage will cause extra power consumption by the CMFB circuit. Decreasing the integration capacitance will decrease the offset charge at the integration capacitance and decrease power consumption of the CMFB circuit. And considering that the power consumption of the CMFB circuit is generally comparable to the bare opamp part, decreasing the CMFB power becomes very important. Another important issue about decreasing the offset charge is that it reduces internal settling by the CMFB circuit and in this way response time of the whole opamp will get better and the opamp can operate at more high frequencies.

IV. Low Power Consumption

At high frequency applications to maintain a reasonable output signal shape, sampling frequency must be increased too. The same amount of increase at the input frequency and the sampling frequency will result in no change of output signals amplitude which can be easily derived in (2). However, increasing the sampling frequency will increase the integration current and integration current can be derived as:

$$I_{\text{int}} = V_{in}.C_s.f_s \tag{14}$$

As can be seen in (14), integration current will increase with increasing sampling frequency. Thus, at high frequencies, current demand of the integrator from the opamp will increase with increasing sampling frequency. With reduced effective input capacitance switched capacitor integrator architecture, effective input sampling capacitance can be reduced which will reduce integration current and which will result in less power consumption.

To show that reduced effective input capacitance switched capacitor integrator is consuming less power, in simulations output stage of the opamp is changed because integration current is provided by the output stage, however decreasing the output stage current gives ability to decrease the intermediate stage(s) current and the input stage current. Thus, power saving by this method can be extended by reducing the other stage currents too.

V. Comparison of Conventional and Reduced Effective Input Capacitance Switched Capacitor Integrator

To test the effectivity of the Reduced effective input capacitance SC Integrator, high frequency input and sampling signals are used. Applied input signal frequency is 100 kHz and amplitude is 100 mV. Sampling signal frequency is chosen as 10 MHz to maintain the input signal shape accurate enough as taking 100 samples in each input signal period. Sampling capacitance of the conventional SC integrator is 1 pF and integration capacitance is calculated as 15.9 pF to obtain 100 mV output signal. Main sampling capacitance of the reduced effective input capacitance SC integrator is again 1 pF and charge sharing capacitance is 9 pF to obtain ten times less current and to obtain ten times less integration capacitance which will result in 1.59 pF. Both integrators are built with TSMC 0.35 μm CMOS transistors in Cadence environment and simulated with spectre. 1 pF capacitance is used for both integrators as load capacitance. Integration current needed for proper integration of the conventional SC integrator is:

$$I_{\text{int}} = V_{in}.C_s.f_s = 0,1.10^{-12}.10^7 = 10^{-6}A = 1\mu A \tag{15}$$

Current needed for reduced effective input capacitance SC integrator is:

$$I_{\text{int}} = \frac{V_{in}.{C_s}^2.f_s}{(C_s + C_{shr})} = 0,1.0,1.10^{-12}.10^7 = 10^{-7}A = 0,1\mu A \tag{16}$$

The current needed for the integration process must be supplied by the output stage of the opamp. Thus, a large integration current needs a large current provided by the opamp. To test the effectiveness of the reduced effective input capacitance SC integrator for low power consumption, different output stage currents are used for simulations. However, results found from the calculations can not be used directly for the simulations; the results are regardless of the quiescent supply current of the output stages, thus the current must be more than this calculated integration currents. Two times of this integration currents will be enough for the quiescent currents of the output stages. Opamp output stages which have 0.2 μA , 2 μA and 20 μA are used for both conventional and reduced effective input capacitance switched capacitor integrator simulations.

VI. Simulation Results

A. Simulation results of 0.2 μA output stage

First, conventional SC integrator and reduced effective input capacitance SC integrator with output stage of 0.2 μA is simulated and settling of the conventional SC integrator is depicted in Figure 6 and reduced effective input capacitance SC integrators settling is depicted in Figure 7. To observe the settling of the integrators, both outputs of each integrator is depicted at the same graph. Expected result from simulation is that, having an offset initially at the output signal of the integrator which means starting with 0 V to 200 mV peak at the beginning of the simulation and settled output must have

zero DC offset and having 100 mV amplitude. As can be seen from the Figure 6 conventional integrator outputs have an increasing offset with the time for both outputs. Also, after some time its DC offset reaches 1.25 V and considering that supply voltage is 1.65 V and threshold of NMOS is 0.5 V and threshold of PMOS is 0.66 V for used technology, output stage transistors goes to linear region from saturation region and this can change the linearity of the integrator. Most importantly, as can be seen from Figure 8 conventional SC integrators outputs phase response is very bad such that output signal can be accepted as sine wave rather than expected cosine. Current needed at the output stage for proper integration for conventional SC integrator is 1 μA and it is obvious that 0.2 μA output stage current will not be sufficient enough for proper integration for the conventional SC integrator.

Reduced effective input capacitance SC Integrators simulation results with output stage of 0.2 μA can be seen in Figure 8 with comparison with the conventional ones results. The settled two outputs of the same reduced effective input capacitance SC integrator with 0.2 μA is depicted at Figure 9. Output signals expected initial amplitude is 200 mV and settled amplitude is 100 mV. As can be seen in the figures, its initial amplitude is almost 60 mV ignoring the 5 mV offset of the opamp. Settled amplitude is almost 30 mV and has roughly 25 mV DC offset at each output. Its worth to mention that slew rate improvements can further enhance the output amplitude very much and slew rate improvement architectures are not used in integrator architectures for this work to see the bare comparison results. The reduced effective input capacitance SC integrator with 0.2 μA output stage has a little phase shift and probably it would not harm the phase response. This reduced effective input capacitance SC integrator with 0.2 μA output quiescent current can be used as an integrator with some adjustments. First, load capacitance can be reduced, because the circuit which will connect to this integrator output will most probably not have 1 pF capacitive load. Second, integration capacitance can be adjusted to get the desired amplitude. 1.59 pF integration capacitance is replaced by 0.5 pF and load capacitance is replaced with 0.1 pF and the two outputs of the adjusted reduced effective input capacitance SC integrator with 0.2 μA can be seen in Figure 10. Conventional SC integrator is adjusted and simulated again too. Integration capacitance is replaced with 5 pF and and load capacitance is replaced with 0.1 pF however, results were almost the same.

B. Simulation results of 2 μA output stage

Second simulation is performed with 2 μA output stages. Conventional SC Integrators settling can be seen in Figure 11. It can be seen that its settling takes almost 10 ms. In Figure 12, reduced effective input capacitance SC integrators settling can be seen. It can be noticed that settling time of reduced effective input capacitance SC integrator with output stage of 2 μA is less than 0.2 μA output stages settling time. Having more current provided by the opamp and increasing of the slew rate makes settling shorter. Settled output of both conventional and reduced effective input capacitance SC integrators can be seen in Figure 13. Reduced effective input capacitance SC integrator is settled having almost 75 mV amplitude ignoring the 5 mV DC offset of the output stage. Conventional SC integrator output has roughly 70 mV having a DC offset addition to the self offset of the opamp. It can easily be said that these two integrators are working correctly however, the output of the conventional one has internal settling oscillation noise. To remove the noise, output capacitance must be increased however, then output amplitude will be affected with this big capacitive load and it will need more power for this extra load. As can be seen from the Figure 13 reduced effective input capacitance SC integrator has no phase shift and conventional ones phase shift is very little.

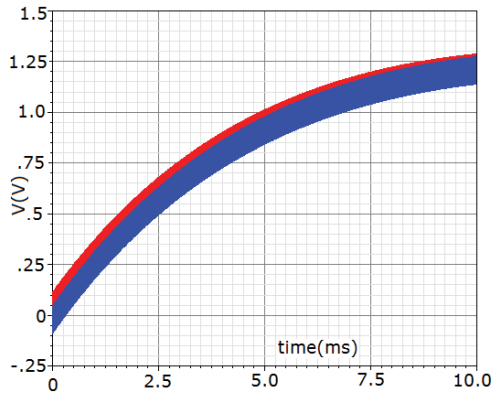

Fig. 6. Settling of Conventional SC integrator with 0.2 μA output stage

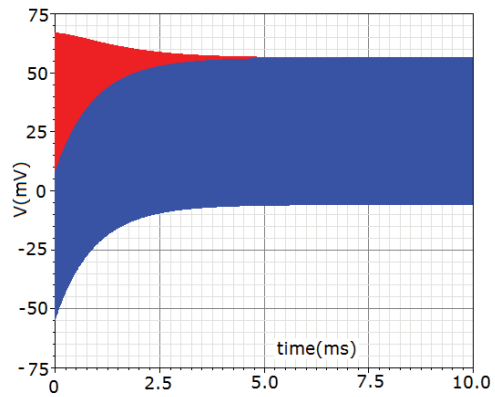

Fig. 7. Settling of Reduced effective input capacitance SC integrator with 0.2 μA output stage

C. Simulation results of 20 μA output stage

Final simulation is done with both integrators with 20 μA output stage. In Figure 14 settling of the conventional SC integrator can be seen. Settling time is decreased compared to 2 μA output stage. In Figure 15 settling of the reduced effective input capacitance SC integrator can be seen. As can be noticed from the figures, settling is reduced with the increasing of the output stage current from 0.2 μA to 2 μA and to 20 μA. In Figure 16, settled output of the conventional and reduced effective input capacitance SC integrator can be seen. As can be seen from the Figure 16 reduced effective input capacitance SC integrator amplitude is slightly more than conventional ones and output signal has not internal

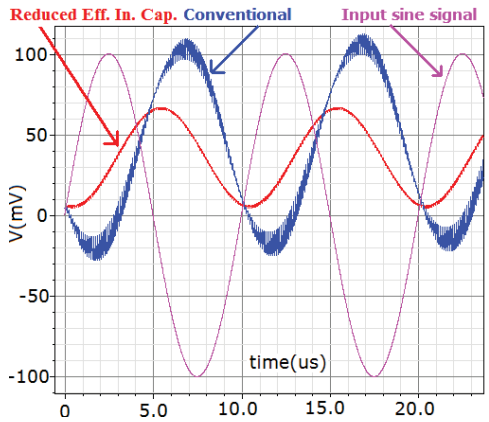

Fig. 8. Beginning of integration with 0.2 μA output stage

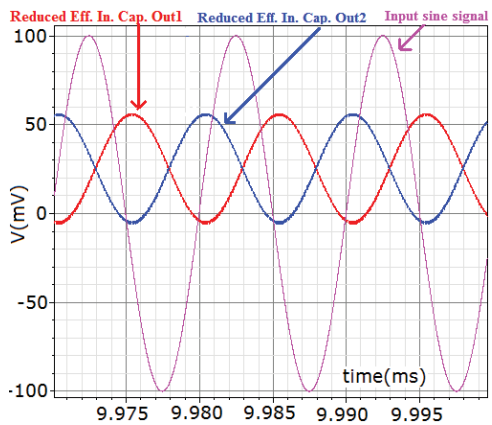

Fig. 9. Settled outputs of Reduced effective input capacitance SC Integrator with 0.2 μA output stage

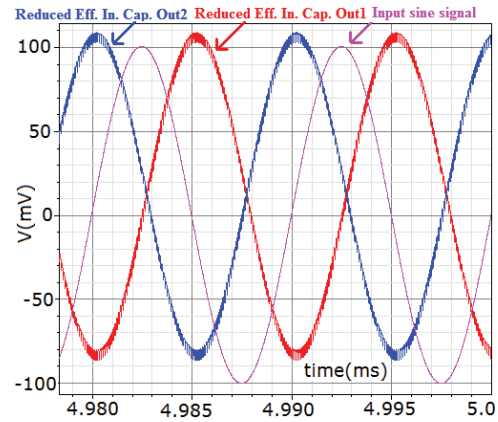

Fig. 10. Settled outputs of adjusted Reduced effective input capacitance SC Integrator with 0.2 μA output stage

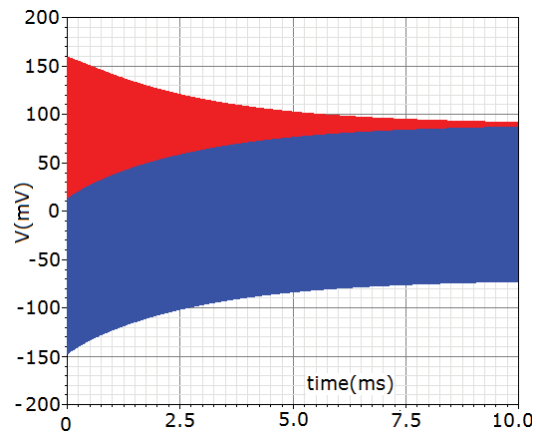

Fig. 11. Settling of Conventional SC integrator with 2 μA output stage

oscillations like the conventional ones and both have almost 85 mV amplitude.

VII. Conclusion

Reduced effective input capacitance Switched Capacitor Integrator is investigated in this work and as can be seen from simulations, this architecture can be used in low power switched capacitor integrators and very large time constant integrators with less power consumption and less die area. Reduced effective input capacitance Switched Capacitor Integrators features can be summarized as:

- Reduced effective sampling capacitance
- Reduced integration capacitance
- Less power consumption
- Reduced settling time
- Stray insensitive
- Less phase error
- Less chip area
- Less internal integration signal settling
- Very useful for very large time constant integrators
- It can be used for less charge injection and clock feedthrough error
- Reduced offset error at the integration capacitance

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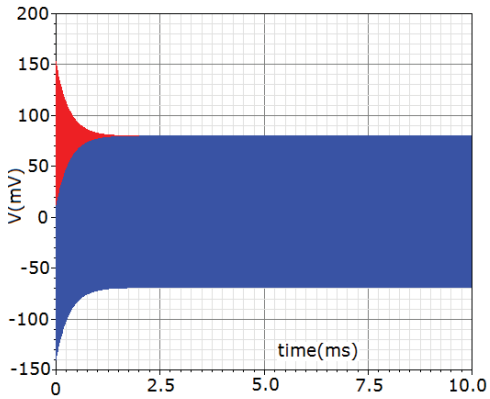

Fig. 12. Settling of Reduced effective input capacitance SC integrator with 2 μA output stage

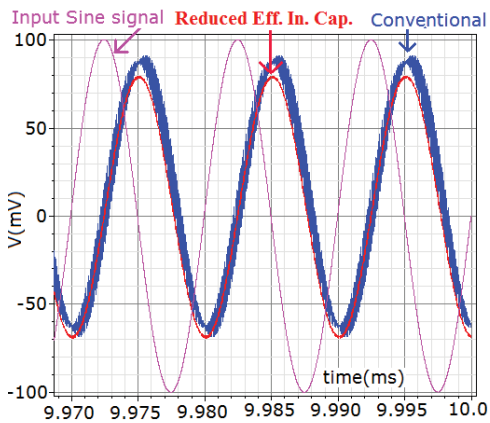

Fig. 13. Settled output of Conventional and Reduced effective input capacitance SC Integrator with 2 μA output stage

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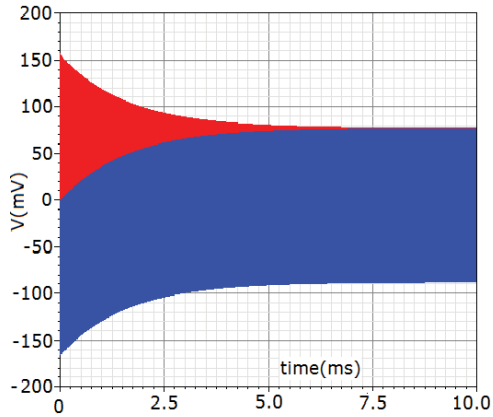

Fig. 14. Settling of Conventional SC integrator with 20 μA output stage

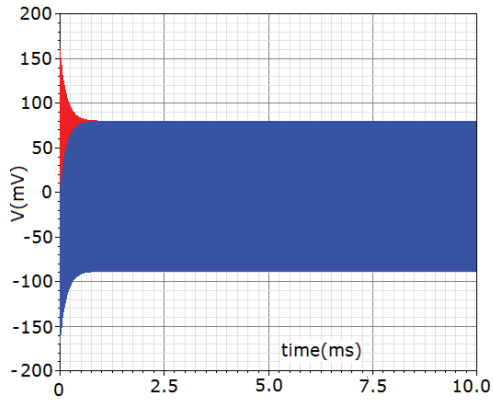

Fig. 15. Settling of Reduced effective input capacitance SC integrator with 20 μA output stage

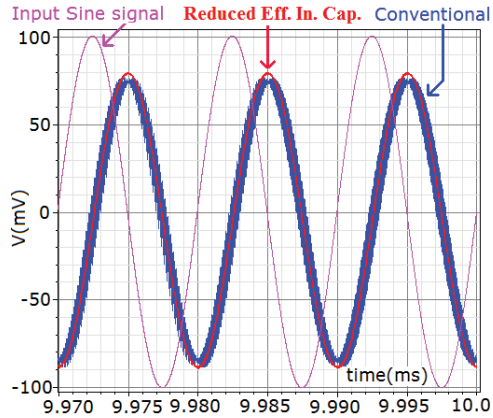

Fig. 16. Settled output of Conventional and Reduced effective input capacitance SC Integrator with 20 μA output stage