A MOSFET only, Step-Up DC-DC Micro Power Converter, for Solar Energy Harvesting Applications

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***Abstract*—In this paper, a step-up micro power converter for solar energy harvesting applications is presented. The circuit is based on a switched-capacitor voltage doubler architecture with MOSFET capacitors, which results in an area approximately eight times smaller than using MiM capacitors for the 0.13 μm CMOS technology. In order to compensate for the loss of efficiency, due to the larger parasitic capacitances, a charge reutilization scheme is employed. The circuit uses a phase controller, designed specifically to work with the series of two PV cells, in order to regulate the output voltage to 1.2 V. Electrical simulations of the circuit, together with an equivalent electrical model of a PV cell, show that the circuit can deliver a power of 536.1 μW to the load, while drawing a power of 799.8 μW from two PV cells stacked in series, corresponding to a maximum efficiency of 67%.**

***Index Terms*—CMOS circuits, electronics, energy harvesting, power management circuits, PV cells.**

I. Introduction

THE ability of an electronic circuit to operate using energy obtained from its surrounding environment can enable the circuit to operate permanently, without the need to be connected to the power grid. This ability is very important for electronic systems that are deployed to locations where it is difficult to connect to the grid, or even to replace their batteries as often as needed. In these situations, an energy independent system with lower installation and operation costs can offset the extra cost of the energy harvesting function and open new application possibilities [1], [2].

Energy can be harvested from different sources, such as: light (solar or artificial), mechanical (usually vibrations), thermal gradients, or electromagnetic [3]. Each one of these energy sources has its own advantages and drawbacks, but they all share a common limitation: low energy density. This means that the available power for a small energy harvesting powered system will be limited. Amongst of all of these sources, ambient light has the highest energy density when compared to other possible ambient energy sources [3], [4]. Ambient light also has the advantage that it can be directly converted into a DC voltage, using a photovoltaic (PV) cell, which simplifies the design of the power converter circuit.

A PV cell is basically a photodiode, whose structure can be built using a CMOS process [5], opening the possibility of integrating in the same silicon die both the power source and the system. The power available from a PV cell depends upon its area and the intensity of the incident light. The voltage produced by a single PV cell (or two cells in series), under load condition, is low and can vary with the light and load variations. As such, it is necessary to have a step-up converter to increase this voltage, and a regulator circuit to produce a stable output voltage with the necessary value for the circuits in the system (e.g. ADCs or DACs) to work. Since both the available power and the available die area are at a premium, the power converter should be as efficient as possible and occupy as little area as possible. The output voltage of the power converter should be stable and independent of load or input voltage variations.

There are two schemes in which a regulator circuit can operate. In the first one, like the one presented in this paper, the PV cell is directly supplying the load, delivering only the needed power. In this case, the PV cell must be able to supply all the power required by the load and the system circuitry. In the second one, it is tried to harvest as much energy as possible out from the PV cell by using an MPPT approach, and to store this energy in a battery or in a super-capacitor.

This paper presents a voltage step-up power converter using MOSFET transistors only. This circuit uses an asynchronous state machine to produce a variable frequency clock that regulates the output voltage to a constant value, independent of the power delivered to the load. The variation (or ripple) in the output voltage is determined by an output capacitor and can be very small if a large capacitor is used. Electrical simulations of the circuit show that it can maintain an output voltage of 1.2 V on a load dissipating 536.1 μW of power, when connected to two PV cells stacked in series, supplying a maximum power of 799.8 μW with an input voltage of 753.8 mV. This yields a maximum efficiency of 67%.

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II. System Architecture

A. Circuit Concept

A simplified schematic of the step-up converter circuit is depicted in Figure 1.

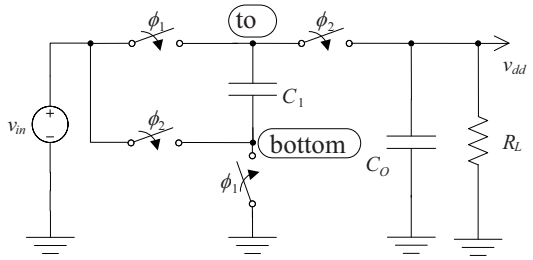

Figure 1. Simplified schematic of the step-up converter.

The principle of operation of the circuit is that of the capacitive voltage doubler [6]: during phase ϕ_1, capacitor C_1 is charged with the input voltage value and then, during phase ϕ_2, it is connect in series with the input voltage source, resulting in an output voltage (v_{dd}) that is two times larger than the input voltage value. Assuming that the output of this circuit is connected to a load resistance (R_L) in parallel with a large external capacitance C_o, the resulting equivalent circuit consists of a voltage source (with a voltage value equal to $2 \cdot v_{in}$) in series with two impedances. The first one is the equivalent impedance of the switched-capacitor and the second one is the load resistance. The average output voltage of this circuit is the voltage division of $2 \cdot v_{in}$ by the resistive divider formed by these two impedances. The output voltage will have a ripple that is inversely proportional to the value of C_o. The value of this capacitance will regulate the upper limit of the output voltage ripple, being inversely proportional to it.

The output voltage value can be regulated by adjusting the value of the equivalent impedance of the switched capacitor. This is done by dynamically changing the frequency of the clock signals that control the switches of the circuit. This change is achieved by an asynchronous state machine (ASM) phase controller.

Any real implementation of the previous circuit is plagued by a parasitic capacitance in the bottom plate node. The capacitance is charged up to v_{in} during phase ϕ_1 and discharged during phase ϕ_2. This is equivalent to a resistance that dissipates energy, thus lowering the efficiency of the circuit. This problem can be particularly serious if MOS capacitances are used, because of the large parasitic capacitance value they introduce. In order to improve the efficiency, it is necessary to reduce the amount of charge that is lost in the parasitic capacitance. This is achieved by splitting the capacitance in two and duplicating the circuit, resulting in an operation with the double of the frequency. Now, the circuit can have a third phase, where the bottom plate nodes of the two half-circuits are connected together, thus transferring half of the charge in one parasitic capacitance to the other, before shorting the first bottom node to ground. This reduces the amount of lost charge by half in the parasitic capacitance nodes. This circuit is depicted in Figure 2. In here, $C_{p\{1,2\}}$ stand for the parasitic capacitance at the bottom plate nodes of each of the MOS capacitors, M_1 and M_2, respectively. This capacitance is constituted by $(C_{db} + C_{sb})$.

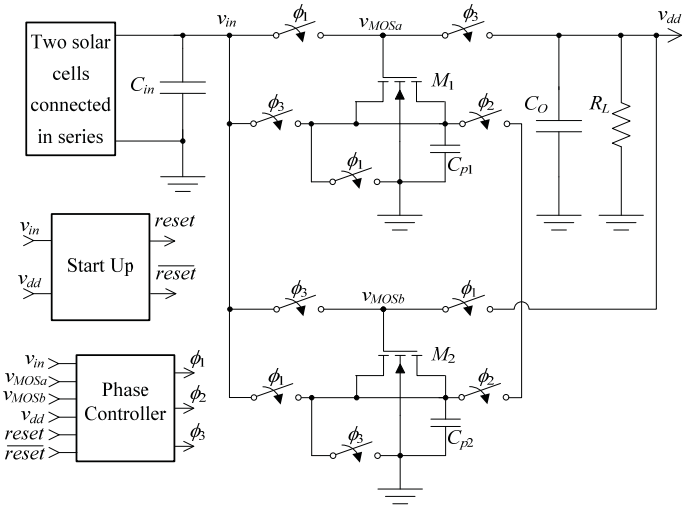

Figure 2. Complete schematic of the proposed step-up converter.

Since both MOS capacitors have the same area, it will be considered that both parasitic capacitances have the same value. Considering ideal voltages and operation, M_1 and M_2 will alternate their role: when ϕ_1 is active, M_1 and C_{p2} are connected in parallel with the input voltage, putting M_2 in series with the input voltage, achieving the voltage doubling at the output, v_{dd}. During this time interval, C_{p1} is discharged, as both of its plates are grounded. When ϕ_3 is active, M_2 and C_{p1} change role with M_1 and C_{p2}, leading to the same behavior that took place when ϕ_1 was active. When ϕ_2 is active, C_{p1} and C_{p2} are connected in parallel, accomplishing a charge distribution between these two parasitic capacitances. Due to the fact that one of these capacitances is charged to v_{in} while the other is completely discharged, when they are connected together, the charge is equally divided, and each capacitor will have half of the charge of the capacitor that was charged to v_{in}. Ideally, the voltage across this parallel circuit will be $v_{in}/2$. By doing this, when the circuit returns to ϕ_1 or ϕ_3 (depending on which was first), the parasitic capacitor that will "steal" charge from the input voltage will be already pre-charged to half of this voltage value. This leads to a lower waste of charge, coming from the input (PV cell), since half of the charge that would be lost is already present.

B. Generation of the clock phases

The state diagram of the ASM is shown in Figure 3. The state machine for the phase controller has four states. Each of these states determines which clock phase is active. The time needed to charge the capacitance M_1 (state1, phase ϕ_1 active) depends upon the maximum current available from the PV cell and on the *RC* time constant of the switches and capacitor M_1. Since this time can change with the available light, a minimum time span, for each state, must be adjusted. The minimum

duration for phase ϕ_1 is given by the time needed to charge M_1 up to 90% of v_{in}, which is a voltage named v_B. This is determined by comparing the voltage of the top plate node of M_1 (which is named v_{MOSa}) to v_B. The output voltage decreases slowly because of the large value of the output capacitance C_o. When v_{MOSa} is larger than v_B, and when the output voltage is smaller than a reference value, phase ϕ_3 must be activated in order to connect M_1 to the output node, thus transferring its charge to C_o and restoring the output voltage value.

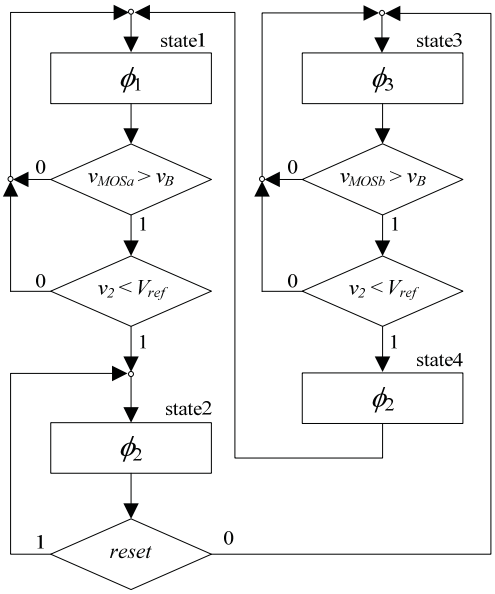

Figure 3. State diagram of the state machine for the phase controller.

The transition from state1 to state3 occurs having state2 in between. In this state, capacitor C_{p1} (which was fully discharged) is connected in parallel with C_{p2}, replenishing the charge of C_{p1} by connecting this capacitance in parallel with C_{p2} (which was charged up to v_B), thus obtaining half of C_{p2} charge. This is done by activating phase ϕ_2.

In state3, capacitors M_1 and M_2 exchange their role, and the circuit behaves like in state1, except for the fact that the main (and the parasitic) capacitances are swapped. Also, instead of considering v_{MOSa}, it should be considered v_{MOSb}. This voltage is the counterpart for v_{MOSa} in the lower half of the circuit depicted in Figure 2. Before changing from state3, back to state1, the state machine goes through state4, in order to activate ϕ_2 with the same purpose as described before, but with the parasitic capacitance roles exchanged between them. In the beginning of each state, it is necessary to introduce a delay before performing any comparison between any two voltages, allowing for the parasitic capacitance charges at the bottom plate nodes of M_1 and M_2 to settle before proceeding.

The circuit of the ASM phase controller is shown in Figure 4. The four states of the circuit are determined by the output of four latches. When the *Set* signal of one latch is active (this can depend on the result of a voltage comparison), the output of the latch changes from 0 to 1. This, in turn, activates the *Reset* signal of the previous latch, causing its output to change from 1 to 0, thus completing the change from one state to the next. There is a delay circuit after each latch, in order to prevent a premature change to the next state. A *reset* signal guarantees that during start-up, the ASM is at state2. The reference voltage, V_{ref}, is an absolute voltage and it must be generated by a bandgap circuit such as the one described in [7]. This circuit needs less than 1 μA to work.

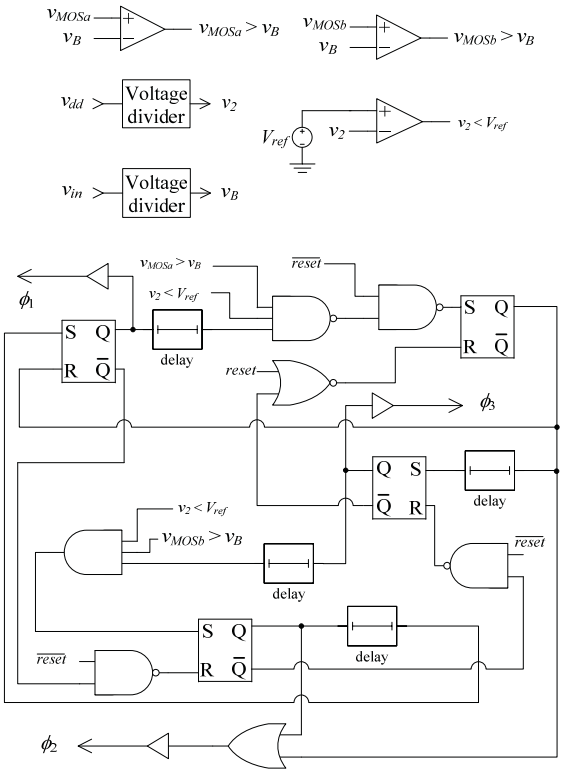

Figure 4. Phase controller schematic.

The v_B reference voltage is obtained by applying the input voltage (v_{in}) to a voltage divider with the ratio of 9 out of 10. The output voltage (v_{dd}) also undergoes a voltage divider, obtaining v_2, which is half v_{dd}.

The schematic of the delay circuit is shown in Figure 5.

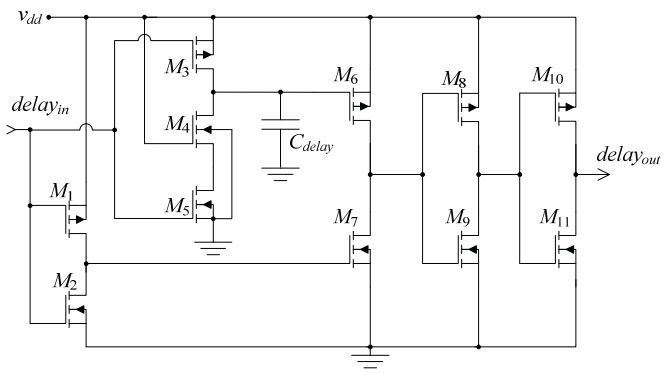

Figure 5. Schematic of the delay circuit.

This circuit delays the rising edge of its input signal. The amount of delay is controlled by the time constant formed by C_{delay} and the R_{DS} resistance of transistor M_4 (which operates in the linear region). Most of the transistors in this circuit, as well the transistors in the ASM circuit, are designed to the

minimum size allowed by the technology, in order to reduce the power dissipation of the phase controller circuit and thus, improving the efficiency. The circuit only uses transistors with larger sizes where the drive capability of the gates is important, such as for the phase buffers.

The schematic of the comparator circuit is shown in Figure 6.

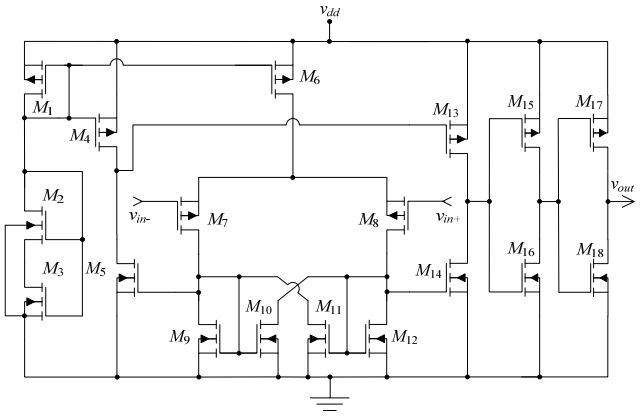

Figure 6. Schematic of the comparator circuit.

This comparator circuit is composed by a PMOS differential pair with a positive feedback load, in order to obtain a large voltage gain with a low power supply voltage value and thus, reducing the systematic offset. This stage is followed by three gain stages to increase the overall gain in order to saturate the output voltage to an unambiguous logic level. These comparators are self biased using a PMOS and a NMOS transistor connected in diode. Each comparator draws a DC current of approximately 8 µA from the power supply.

III. Simulation Results

In order to verify the functionality of the step-up converter, the circuit was designed in a 0.13 µm CMOS technology and simulated using Spectre. The option of using MOS capacitors allows obtaining an area eight times smaller than the one that would have been if the capacitors implemented by M_1 and M_2 were implemented with MiM capacitors instead. The estimative for the area of M_1 is 416000 µm^2, but if a MiM capacitor was used instead, this area would increase to 3300000 µm^2, for the same value of capacitance.

The schematic of the start-up circuit is depicted in Figure 7.

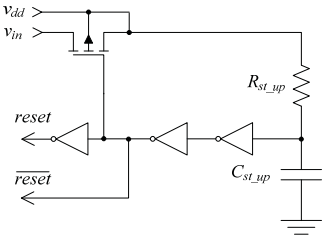

Figure 7. Start-up circuit schematic.

This circuit shunts the input and the output nodes during the start-up of the circuit, guaranteeing that the phase controller circuit has a high enough power supply voltage to start working. This circuit also provides the *reset* signal, and its complement, for the ASM.

A. PV cell equivalent circuit

The PV cells described in [5], have an open circuit voltage of around 470 mV, which is a value too low to use with a voltage doubler circuit, requiring a step-up converter capable of multiplying by 3. Given that the desired output voltage is low (1.2 V), this type of converter would have a very low efficiency [6]. Therefore, it is preferable to use two PV cells in series, in order to obtain an open circuit voltage of around 920 mV. Using the measurement data from [5] it is possible to extrapolate that a PV cell with 3 mm^2 would produce around 390 µW and would have a short circuit current of 1.62 mA. A PV cell can be modeled by an equivalent electric circuit, shown in Figure 8. The values of the parameters of the equivalent circuit (I_S, R_P and R_S) are adjusted to match as best as possible the extrapolated data for the PV cell.

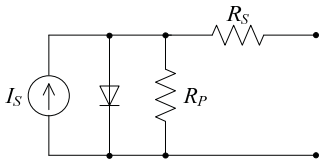

Figure 8. Equivalent electrical circuit of a PV cell.

Two PV cells in series (each having 3 mm^2) are simulated using two equivalent circuits in series, resulting in the power curves depicted in Figure 9.

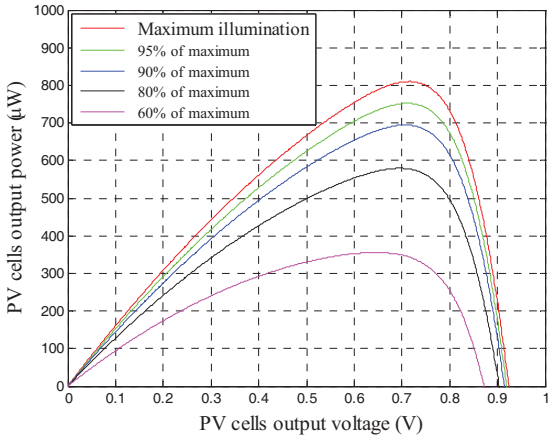

Figure 9. Power curve of two PV cells equivalent circuits connected in series, for different levels of illumination.

In here, one can depict the PV cells output power functions for some levels of light intensity, namely, for 100%, 95%, 90%, 80% and 60% of the maximum illumination.

The maximum available power at the output will be in accordance to the light intensity to which the cell is subjected. The information about the maximum power available from the PV cells, as well as the voltage at which that maximum power occurs, the short circuit current and the open circuit voltage, is summarized in TABLE I.

TABLE I. PV CELLS ELECTRICAL CHARACTERISTICS FOR DIFFERENT LIGHT INTENSITIES

Light Intensity	P_{max} (µW)	v_{max} (mV)	I_{SC} (mA)	V_{OC} (mV)
100%	810.1	718.9	1.680	924.1
95%	752.2	710.0	1.596	919.6
90%	694.4	709.9	1.512	914.7
80%	579.3	699.7	1.344	903.6
60%	355.5	648.6	1.008	872.1

B. *Electrical simulations of the system*

To note that all simulations referred in this sub-section were performed considering the maximum light intensity, i.e. at 100%.

The step-up converter was designed to work with two PV cells in series, supplying a maximum power of 810 µW and occupying a total area of 6 mm^2. The electrical simulations of the system show that it achieves the correct output voltage value when there is no load connected to its output node. It is not possible to have a significant load connected to the circuit during start-up because the PV cells cannot provide enough energy to charge the output capacitor and supply the load at the same time. The evolution of the input and output voltages during start-up is shown in Figure 10.

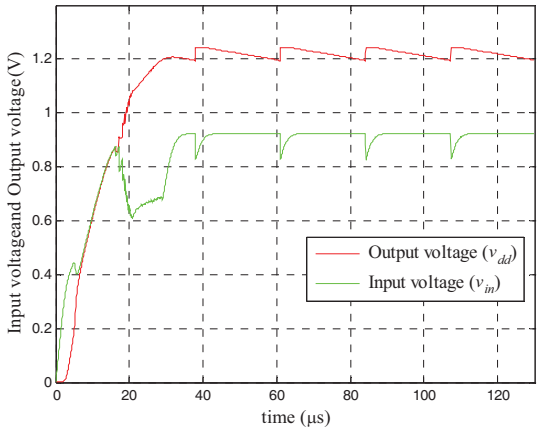

Figure 10. Evolution of the input and output voltages during start-up.

After the circuit achieves the desired output voltage value and enters a steady state, it is possible to connect a higher load to the output. By changing this load value it is possible to see that the circuit dynamically adjusts the phases in order to maintain an output voltage value of 1.2 V.

The power dissipation of the circuit (total power supplied by the PV cells) increases with the clock frequency (and with the load power). The efficiency and power values of the circuit for different load power values are shown in Figure 11.

This graph shows that the maximum efficiency of the circuit is 67% for a power delivered to the load of 536.1 µW and a total circuit power dissipation of 799.8 µW, which is very close to the maximum available power from the two PV cells. From a theoretical point of view, as stated in [6], the maximum achievable efficiency of an ideal converter with an input voltage of 753.8 mV and an output voltage of 1.2 V (which are the average values of v_{in} and v_{dd} in this situation, respectively)

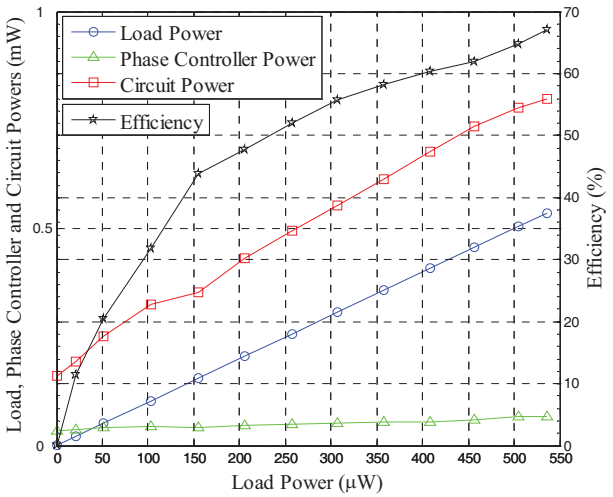

Figure 11. Efficiency, input power, output power and phase controller circuit power, as a function of the power delivered to load.

would be 79.6%. The phase generator circuit only dissipates 67.2 µW. The frequency of the clock phase ϕ_1 under this load condition is 666.4 kHz. In order to understand how much is the efficiency penalty of using MOS transistors, instead of MiM capacitors, a simulation where the MOS transistors were replaced by MiM capacitors of the given technology was performed. In this case the maximum efficiency increased to 68.23%, which is not significant, given the die area tradeoff.

In [8], the results that were obtained for the maximum efficiency, regardless of the approach that was taken, yielded similar results to the ones presented in this paper.

The operating frequency for phase ϕ_1, as a function of the load power is shown in Figure 12. As expected, as the load power increases, so does the operating frequency.

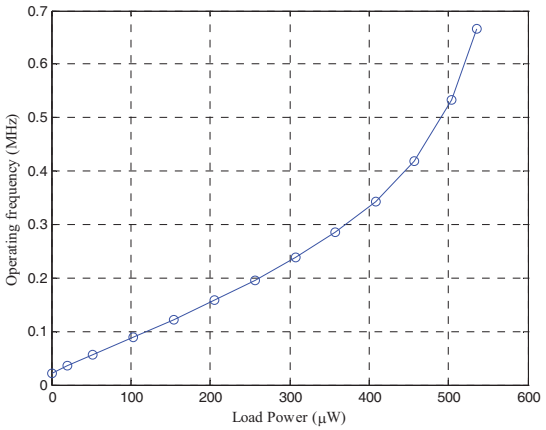

Figure 12. Operating frequency (ϕ_1) as a function of the load power.

The results that produced the best efficiency were obtained with the circuit operating near the maximum power point of the PV cells. However, this efficiency is only possible when the load connected to the output of the circuit, together with the control circuitry, dissipate a power close to this power level. This circuit was designed to operate under a favorable situation of maximum illumination.

The evolution of the average input and output voltages, as a function of the load power is depicted in Figure 13. It can be

seen, that across the range of the load power, the output voltage is approximately the same, as the circuit is made to regulate the output voltage to approximately 1.2 V. This graph also shows that when the load power increases, the PV cells output voltage decreases and becomes closer to the maximum power point voltage of the PV cells.

A performance metric of the circuit is the energy per cycle, as a function of the load power. This function is depicted in Figure 14.

In order to check the robustness of the regulator circuit when experiencing a sudden load change, Figure 15. shows how the circuit behaves under a load-transient operation, when asked to supply a load demanding 80% and 20% of the maximum achievable power at the output.

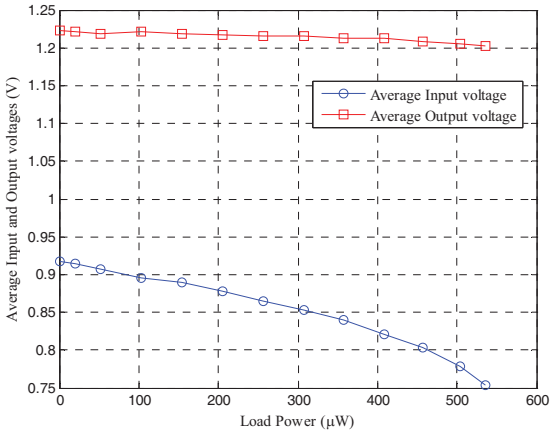

Figure 13. Average circuit input and output voltages, as a function of the load power.

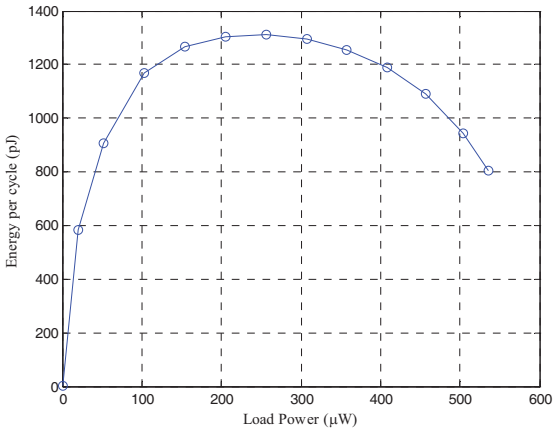

Figure 14. Energy per cycle as a function of the load power.

The load demanding 20% of the maximum power was present from 0 until 10 μs, 40 μs to 70 μs and 100 μs to the end of the simulation. The load asking for 80% of maximum power was present during the complementary intervals. Clock signal ϕ_1 is also shown, increasing its frequency when a larger output power is required. The ripple in the output voltage is due to using an output capacitor of only 10 nF, due to simulation time restrictions. If a larger capacitor was used, for example 100 nF, the ripple amplitude would be divided by 10.

C. Electrical behavior with illuminations different from maximum illumination

The circuit was simulated using different illuminations over the PV cells. Since the objective of the circuit is to regulate the output voltage, it can only work if the available power from the PV cells is enough to supply the load and the control circuit at the same time. This means that when the illumination is low, the load connected to the circuit must also be low (higher R_L).

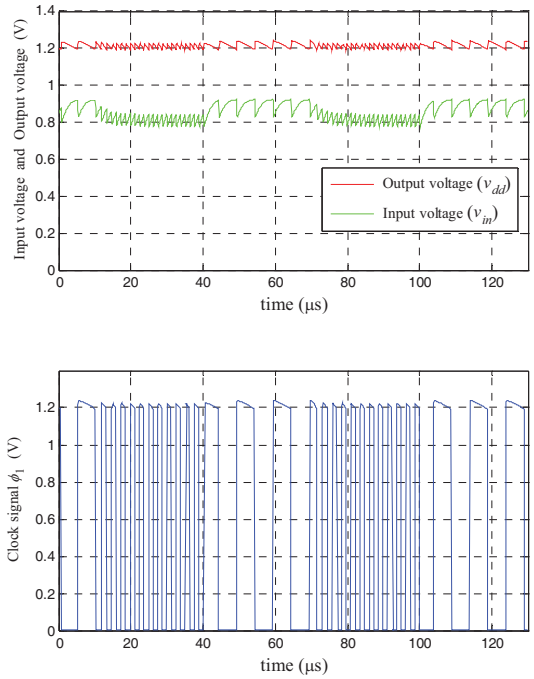

Figure 15. Regulator circuit behavior under load-transient operation (top, v_{in} and v_{dd} voltages; bottom, ϕ_1 clock signal).

During start up, the power needed by the whole circuit increases, because it needs to charge the output capacitor resulting in the circuit maximizing its operating frequency. The start-up of the circuit was simulated for different illumination levels. The start-up was only successful for illumination levels above 80% of the maximum. The evolution of the input and output voltages during start-up, with an illumination level of 80% of the maximum, is shown in Figure 16.

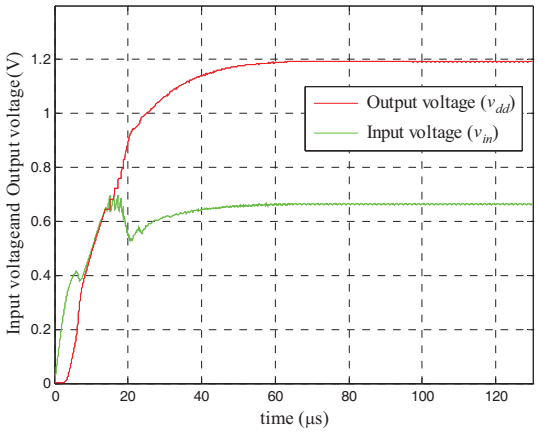

Figure 16. Evolution of the input and output voltages during start-up, with 80% of the maximum level of illumination.

In this limit situation, the output voltage nearly reaches the desired value, foreseeing that it would not be feasible to connect a load to the output. The power provided by the PV cells is 575.1 µW, very close to the maximum power that the cells can produce for this illumination level, leaving no power left to supply any significant load.

With an illumination of 95% of the maximum, it is possible to start-up in a similar fashion as with full illumination, as depicted in Figure 17.

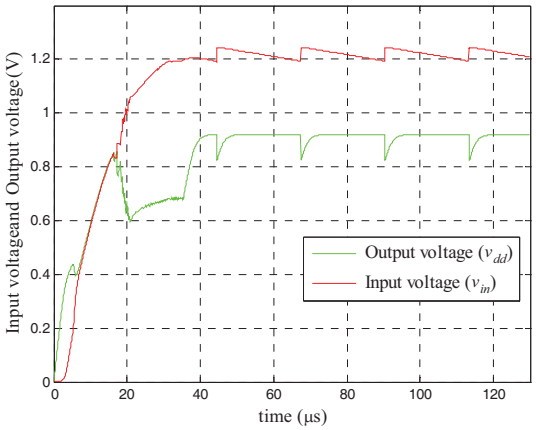

Figure 17. Evolution of the input and output voltages during start-up, with 95% of the maximum level of illumination.

As it would be expectable, the circuit takes more time to reach the steady state than when there is full illumination, because there is less available charge from the PV cells.

It is possible for the circuit to work with illumination levels lower than the maximum level. However, the range of loads connected to the output must be such that the overall system power does not exceed the maximum power provided by the PV cells. Moreover, the system must have previously started-up successfully, which can only be achieved with a significant level of light intensity.

The efficiency and power values of the circuit for different load power values, when the PV cell is under 60% of maximum illumination are shown in Figure 18.

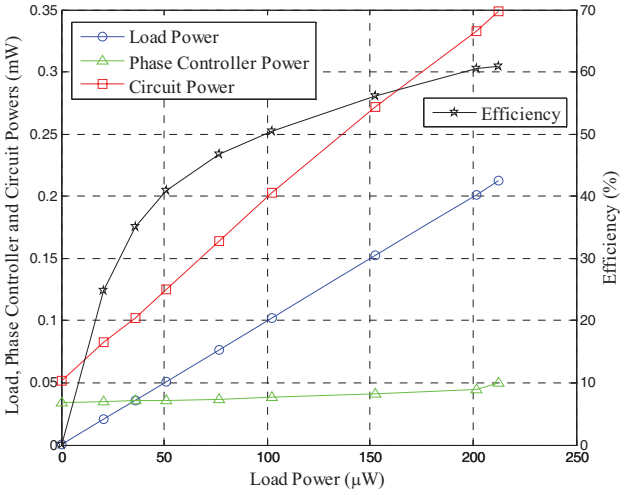

Figure 18. Efficiency, input power, ouput power and phase controller circuit power, as a function of the power delivered to load, when the PV cells experience an illumination of 60% of the maximum.

The maximum efficiency of the circuit under these conditions is 61%, for a power delivered to the load of 212.2 µW and a total circuit power dissipation of 348.8 µW, which, once again, is very close to the maximum available power of the series from the two PV cells (TABLE I.). The phase generator circuit dissipates 50.35 µW under these circumstances, with a frequency value of 470 kHz for the clock phase ϕ_1.

To assess the robustness of the system to different levels of light intensity, the latter was varied between 100% and 60% of the maximum, after system start-up. The load of the system was set at 200µW. This light-transient test is shown in Figure 19.

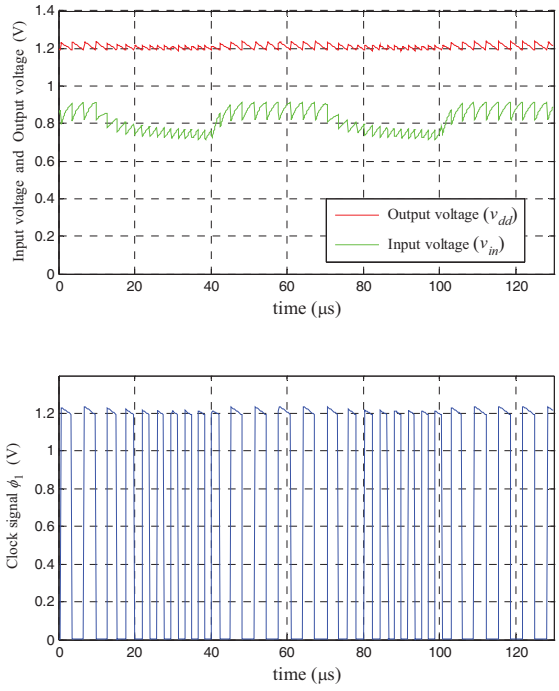

Figure 19. Regulator circuit behavior under light-transient operation using 100% (higher v_{in}) and 60% (lower v_{in}) of maximum illumination (top, v_{in} and v_{dd} voltages; bottom, ϕ_1 clock signal).

The maximum light intensity was present from 0 until 10 µs, 40 µs to 70 µs and 100 µs to the end of the simulation. The 60% of maximum illumination was present during the complementary intervals.

In a light-transient test, such as the one that was performed, if the circuit is asked to supply a load requiring more than the power that the circuit can provide, the output voltage will drop, the switching frequency will rise towards its maximum value (trying to get more electric charge from the PV cells) and the circuit will eventually stop working. The main reason why the circuit will cease working is due to the fact that all powered devices in the circuit depend upon the voltage v_{dd}, in particular, the logic circuits inside the phase generator and controller. The high logic level will get progressively lower, just like the voltages needed to control the MOSFET devices. The available voltages will be unable to turn them ON.

This circuit can still work with weaker illumination, as long as, on one hand, the maximum power of the cells is enough to supply the load at the output (and the control circuits) and, on

the other hand, the voltage at which this power is located in the power function is enough to reach, after being stepped up, in the least, the value of 1.2 V.

One must keep in mind that, as the illumination gets lower, so does the available power to deliver to the output. As such, this will restrict the applicability of the circuit, since it will only be able to supply a narrower range of output loads.

IV. Conclusions

A step-up micro-power converter for solar energy harvesting applications was presented. The circuit is based on a switched-circuit voltage doubler architecture, with MOSFET capacitors, which results in a total circuit area approximately eight times smaller than using MiM capacitors of the given technology. In order to compensate for the loss of efficiency, due to the larger parasitic capacitances, a charge reutilization scheme was employed. The circuit uses a phase controller, designed specifically to work with a series of two PV cells, in order to regulate the output voltage to 1.2 V. Electrical simulations of the circuit, together with an equivalent electrical model of a PV cell show that the circuit can deliver a power of 536.1 μW to the load, while drawing a power of 799.8 μW from the series of two PV cells, corresponding to a maximum efficiency of 67%. When using the MiM capacitors, the increase of efficiency to 68.23% is not significant, considering the eight times less die area tradeoff.

The system shows to be robust enough when illuminated with the maximum level of light, being tolerant to a significant variation of the demanded power at the output.

With a lower light intensity, the range of output power is reduced, only allowing for a stricter range of load resistances, with higher values than those used with maximum illumination. The system must always be started-up with an illumination level of, at least, 95% of the maximum light intensity. After a successful start-up, the light intensity can drop and the circuit can still work, as long as the power required by the output, and the control circuitry together, is within the maximum power that the PV cells can provide for the particular light situation, and as long as the maximum power point voltage of the PV cells is enough to reach 1.2 V after step-up.

References

[1] Paradiso, J.A.; Starner, T., "Energy scavenging for mobile and wireless electronics," Pervasive Computing, IEEE , vol.4, no.1, pp. 18-27, Jan.-March 2005.

[2] Jiang, X.; Polastre, J.; Culler, D., "Perpetual environmentally powered sensor networks," Fourth International Symposium on Information Processing in Sensor Networks, 2005. IPSN 2005, vol., no., pp. 463-468, 15 April 2005.

[3] Chalasani, S.; Conrad, J.M., "A survey of energy harvesting sources for embedded systems," Southeastcon, 2008. IEEE , vol., no., pp.442-447, 3-6 April 2008.

[4] Chandrakasan, A.P.; Daly, D.C.; Kwong, J.; Ramadass, Y.K., "Next generation micro-power systems," VLSI Circuits, 2008 IEEE Symposium on , vol., no., pp.2-5, 18-20 June 2008.

[5] Guilar, N. J.; Fong, E. G.; Kleeburg, T.; Yankelevich, D. R. & Amirtharajah, R. (2008), Energy harvesting photodiodes with integrated 2D diffractive storage capacitance, *in* 'ISLPED '08: Proceeding of the 13th international symposium on Low power electronics and design', ACM, New York, NY, USA, pp. 63-68.

[6] Zhu, G. & Ioinovici, A. (1996), Switched-capacitor power supplies: DC voltage ratio, efficiency, ripple, regulation, *in* 'Proc. IEEE International Symposium on Circuits and Systems ISCAS '96., 'Connecting the World", pp. 553-556.

[7] De Vita, G. & Iannaccone, G. (2007), 'A Sub-1-V, 10 ppm/ºC, Nanopower Voltage Reference Generator', *IEEE Journal of Solid-State Circuits* 42(7), 1536-1542.

[8] Hui Shao; Chi-Ying Tsui; Wing-Hung Ki, "The Design of a Micro Power Management System for Applications Using Photovoltaic Cells With the Maximum Output Power Control," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol.17, no.8, pp.1138-1142, Aug. 2009.

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