

Power Supply Unit for ATCA–based Piezo Compensation System

Konrad Przygoda, Tomasz Pozniak, Dariusz Makowski, *Member, IEEE*, Tomasz Kozak, Marcin Wisniewski, Andrzej Napieralski, *Senior Member, IEEE*, and Mariusz Grecki

Abstract—Pulsed operation of high gradient superconducting radio frequency (SCRF) cavities results in dynamic Lorentz force detuning (LFD) approaching or exceeding the bandwidth of the cavity of order of hundred of Hz. The resulting modulation of the resonance frequency of the cavity is leading to a perturbation of the amplitude and phase of the accelerating field, which can be controlled only at the expense of RF power [1-3]. The X-Ray Free Electron Laser (X-FEL) accelerator, which is now under development in Deutsches Elektronen-Synchrotron (DESY), will consist of around 800 cavities with a fast tuner fixture including the actuator / sensor configuration. Therefore, it is necessary to design a distributed control system which could be able to supervise around 25 RF stations, each one comprised of 32 cavities. The Advanced Telecommunications Computing Architecture (ATCA) was chosen to design, develop, and build a Low Level Radio Frequency (LLRF) controller for X-FEL. The already performed tests of ATCA LLRF control system proofed the possibilities of usage of such a standard for high energy physics experiments [4]. The paper presents the concept of integration of the piezo compensation system to the ATCA standards with special emphasis to the hardware part of the system. Moreover, the first results from carried out tests of the prototype power supply unit for piezo drivers integrated to ATCA board will be presented.

Index Terms—piezo compensation, Lorentz force detuning, power supply unit, ATCA architecture

I. INTRODUCTION

THE large scale accelerator machines as well as detector systems have made use of several generations of modular instrument standards. The standards such as Nuclear Instrumentation Module (NIM), Computer Automated Measurement And Control (CAMAC) and FASTBUS have been used for high energy physics from the latest 60s and processed as open industry standards with IEEE and ANSI in U.S. and the IEC globally. Nowadays, most accelerator control systems are built on Versa Module Eurocard (VME) standard with some migrations to VME eXtensions for Instrumentation (VXI), which is more suitable for better shielding and additional timing and triggering features for high speed instruments. All of these systems have similar very high pin count backplanes, first of all to handle parallel data transfers between data collection and processing modules with the time multiplexed results sent upward through a single crate controller.

Almost decade ago, it was quickly find out that the multiplexed parallel bus architecture would become obsolete as the base technologies for data communications moved ever more strongly toward high speed serial links, especially between devices within a module. The new preferred architecture became conceptually a stand-alone functional module accepting a single voltage power input, analog and digital data inputs, and a timing signal, that transmits out its processed results digitally on a single high speed serial link. In 2004, PICMG consortium started its new design and called it Advanced Telecommunications Computing Architecture (ATCA), mainly due to the fact that it was preliminary dedicated for industries of Telecom and Computing.

Currently, under studies at many laboratories are different architectures for LLRF control system [5-9]. The LLRF control system of Free Electron Laser in Hamburg (FLASH) in DESY or Horizontal Test Stand (HTS) in Fermi National Lab (FNAL) are still based on VME standard. The VXI standard seems to be very attractive solution for multichannel control. The receiver chases comprised of the Multichannel Field Controller Cards (MFC) can accommodate up to 96 channels of the New Muon Lab (NML) facility. Since, the high availability electronics design techniques are becoming standard practice in industries of Telecommunications, the High Energy Physics laboratories rapidly started their investigations on ATCA and μ TCA (MicroTCA) architectures. Collaborators at KEK, FNAL and DESY are leading the ATCA based LLRF control studies [4]. The ATCA and Advanced Mezzanine Card (AMC) standards offer modular design, hot-swapping as well as redundancy. The single ATCA shelf can handle up to 36 superconducting cavities to control the drive to the klystron and maintain its output power amplitude and phase in stable relationship to the beam.

The piezo compensation system is an integral part of LLRF control system of FLASH facility [10]. It is based on VME standard and it is capable of compensating up to 64 cavities simultaneously. The principle of its operation is to measure an accelerating field gradient, forward and reflected power and generates complex signals composed of I (In-phase) and Q (Quadrature) components. The IQ signals are used for cavity detuning computation and compensation pulse parameters estimation [11-13]. The piezo compensation pulse is generated to modulate the cavity resonance frequency using a dedicated power amplifier – piezo driver - and piezoelectric actuator.

K. Przygoda (corresponding author) is with the Technical University of Łódź, Department of Microelectronics and Computer Science, Wólczajska 221/223, 90-924, Łódź, Poland, phone: +48 426312720, e-mail: kprzygod@dmc.pl.

Even reliable and efficient, the existing piezo control system has many disadvantages. From most of all, it is a lack of redundancy circuits, especially for the most important block as power supply unit. The hot-swapping function is also most wanted feature, especially when there is a need to exchange broken part without switching off the main power supply.

Since the single RF station for X-FEL facility will consist of up to 32 cavities and almost 25 RF stations will be placed along the main linac, there is a need to control up to 800 cavities equipped with 1600 piezo fixture tuners. In order to meet such a large scale machine configuration, the ATCA architecture with its modular design, hot-swapping, redundancy for the most crucial circuits as well as single relatively high voltage power bus is proposed.

II. CONCEPT FOR PIEZO CONTROL DESIGN IN ATCA STANDARD

A. ATCA standard overview

The ATCA standard is accomplished with chassis (shelf) cluster concept that is air-cooled, redundant for all main functions (power supply, network, controller, hub switch as well as diagnostic control layer) and scalable to large or small clusters down to a very small payload module. Furthermore, the shelf is hot-swap capable at both the large ATCA carrier blade and smaller Advanced Mezzanine Card (AMC) modules, see Fig. 1. The chassis also includes a backplane for Rear Transition Module (RTM) with IO for ATCA carrier, and separate shelf options for the AMC card called μ TCA (MicroTCA).



Fig. 1. The ATCA shelves for ATCA Carrier boards (left) and μ TCA cards [14].

The ATCA Carrier blade can be used for standalone functionality, however it can be easily extended using AMC modules directly connected to AMC bays. The full size ATCA Carrier board is mainly fulfilled for backplane connections using RTM module. One can distinguish three main Zones used for such a backplane, see Fig. 2. Zone 1 provides connection for redundant power supply bus which is -48 V. Zone 2 is capable of transmitting fast serial data using Dual Star Fabric or even Dual Network Switch Module. Typically, it is used for fast serial links using RocketIO, PCIExpress or even GbEthernet (GbE) interfaces. Zone 3 area can be user defined and it is typically used for various digital and analog fast interconnections via RTM module.

The faceplate of the typical ATCA Carrier board is accomplished with alignment pins, floating fastener, ATCA LEDs with blue one for module activation and deactivation indication as well as handle with intelligent Hot Swap Switch.

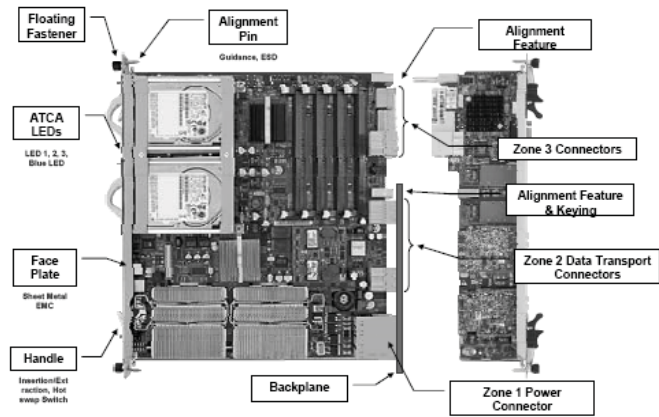


Fig. 2. ATCA carrier blade with Rear Transition Module connected on backplane [15].

Moreover, the backplane side of the Carrier board is supported by alignment features and keying. The ATCA Carrier boards are placed in shelf which is supervised by a Shelf Manager. The Shelf Manager communicates with all ATCA boards, Power Entry Modules, Fan Trays, or other modules through (IPMB-0) - the dual, redundant I²C-based bus, common for all ATCA boards. The Shelf Manager Controller communicates with Module Management Controllers (MMCs) on AMC modules through another I²C-based IPMB-L - the local bus, which connects MMCs with an Intelligent Platform Management Controller (IPMC) on the Carrier Board.

B. ATCA-based piezo control system

The main parts of the piezo control system are driving and sensing circuits. The driving circuits are composed of power amplifiers used for high power signals generation applied to piezo actuator. The power amplifiers are driven with low voltage signals using DAC converters. The sensing circuits are comprised of instrumentation amplifiers for piezo sensor signal conditioning. The closed loop operation of the piezo control is accomplished using ADC converters [16].

The piezo driving circuits were decided to be located on ATCA Carrier board. The number of 16 power amplifiers have been placed as 4x4 matrix located on the center, top side of the ATCA Carrier board, see Fig. 8. The high power output signals from power amplifiers are connected to the Zone 3 connector. The current limitation for each provided signal was doubled using differential pin pairs.

The piezo sensing circuits were moved to RTM module in a case of limited space on the main Carrier board. The faceplate of the RTM module was fitted to handle up to 16 output and 16 input signals. The high power output signals are driven to piezo actuators using coaxial pin of used connectors. The coaxial shield of the connector is used for feedback signal from piezo actuator - voltage and current sense. The same scheme was applied for differential input signals taken from the piezos operated as mechanical vibration sensors.

The power supply unit applied for piezo driving circuits was integrated into ATCA carrier and it is located close to Zone 3 area. The input power payload of -48V is converted to

±85V using dedicated DC/DC converters connected in series. The main payload of -48V is converted to 12V using a dedicated ATCA DC/DC buck converter and next provided for corresponding (Low-dropout) LDO regulators. The output voltage of each LDO is monitored and can be switched on and off by IPMC controller placed on the ATCA carrier blade.

The FPGA device is responsible for real time computations as well as control of the DAC and ADC converters. The FPGA device is supported by built in fast serial links such as RocketIO and SGMII that are used for communication with outside world. The RocketIO interface is connected to hardware cross-switch device for full mesh configuration. It allows piezo control board connection to the first 10 slots of ATCA shelf. The SGMII interface is used for communication with external device which provides physical layer for GbEthernet interface. The GbE#1 interface is connected to Zone 2 connector and it is treated as a redundant communication channel with other ATCA boards. The GbE#2 interface is placed to the front panel and it is planned to be used for fast debugging purpose of the crucial components. The TCP/IP stack implementation for embedded systems is supported by Lightweight IP (lwIP) open source code. Xilinx Embedded Development Kit (EDK) provides lwIP software customized to run on Xilinx Embedded systems containing either a PowerPC or a MicroBlaze processor [18]. The functionality of the IPMC is fulfilled by a dedicated microcontroller with 6 built-in I²C interface bus drivers. It allows to eliminate the usage of I²C interface bus expanders. The IPMC is responsible for buffering of the incoming IPMI messages, processing them and for generating appropriate IPMI response messages, when necessary. Furthermore, the IPMC controls the whole process of Field Replaceable Unit (FRU) activation and deactivation, when the Carrier board is inserted into, or extracted from the chassis. The IPMC provides also the Shelf Manager with the information concerning the whole board (FRV Repository) and all sensors (Sensor Data Records) [17]. What is more, the role of the

IPMC is to control the most important modules such as power supply units and communication with MMC placed on the Rear Transmission Module. When the RTM module is connected or disconnected from the ATCA Carrier board, the MMC is sending a proper message to IPMC and the high voltage power supply is switched off or on. The block diagram of the proposed ATCA-based piezo control system is presented in Fig. 3.

III. POWER SUPPLY UNIT FOR ATCA-BASED PIEZO COMPENSATION SYSTEM

The most important circuit of the ATCA piezo board is power supply unit that is provided to supply the power amplifiers – piezo drivers. It should provide a very stable voltage, since any ripples on the power supply can disturb the piezo driving signal and results on unexpected accelerating field errors. Since the piezo elements are capacitance load of order of 5 μF and they need a power signals of 100 V and frequency of 300 Hz (main mechanical resonance frequency of sc cavity), the average peak current for single power amplifier is close to 1 Amp. The power supply current for 8-channel piezo drivers loaded of 5 μF capacitance load was measured to be 0.3 Amp. According to the specified load and driving signal requirements, the power supply unit of output power of more than 100 W should be considered. The DC/DC converters from Vicor were taken into consideration to build a desired power supply unit. The VTM, PRM and BCM single chip devices have been chosen according to the main ATCA power supply unit of -48 V. The main parameters of chosen models are collected in Tab. 1.

TABLE I. DC/DC CONVERTERS FROM VICOR

Parameter	PRM P048F048T24AL	VTM V048F480T006	BCM B048F48T30
V _{in} [V]	48 (36÷75)	48 (26-55)	48 (38-55)
V _{out} [V]	48 (26÷55)	48 (26-55)	48 (38-55)
P _{out} [W]	240	336	300
η [%]	96	96	>96

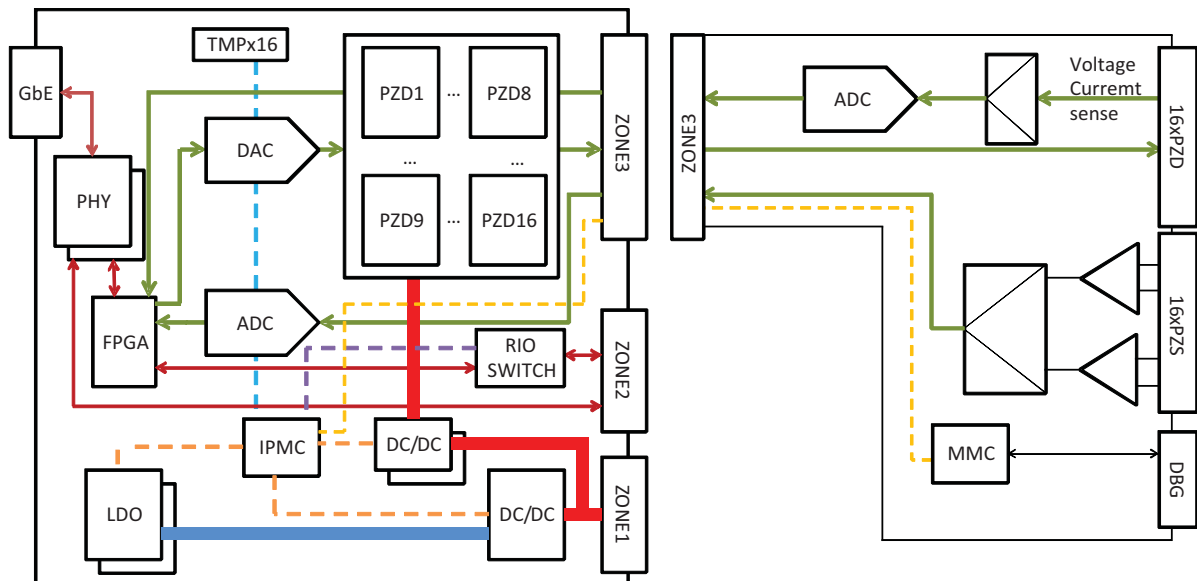


Fig. 3. The block diagram of ATCA Carrier board (left) for piezo compensation with RTM module (right).

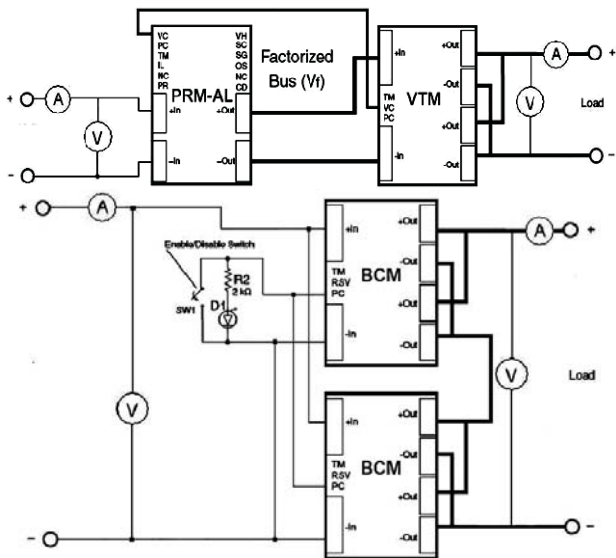


Fig. 4. The block diagram of tested DC/DC converters. The top topology is used for PRM-VTM chips, the bottom topology is used for BCM chips [19].

The each DC/DC converter was tested independently and next the various configurations of used models were investigated. The measurement circuits are presented in Fig. 4. The PRM and VTM devices can be used as independent DC/DC converters. However, the series connections of such devices is strongly recommended by Vendor. The most important is VC control voltage that should be connected from PRM output to VTM input pin. The VC voltage should be equal or more than 14 V and it should be kept constant as long as possible for continuous and reliable operation of converter. The PC open collector pin presented on the both devices should be unconnected or connected to 2.4 V for output voltage activation. The PRM-VTM DC/DC converter was loaded with different resistance and next the typical characteristics were measured. It is clearly visible that the efficiency of the device under test (DUT) is closed to 90% for load of 33 Ω and nominal input voltage range of 48V. Since, the nominal power supply voltage for piezo drivers is experimentally estimated to be $\pm 100V$, the VTM-PRM devices should be connected for the primary side parallel and for secondary side in series. It gives around 16 of such device to meet such a requirement. Moreover, the possibility of VC control voltage loss cannot be accepted for reliable operation of piezo compensation system. Therefore, the BCM converters have been investigated. The BCM DC/DC converter can be used independently for building a sophisticated power supply units. The fact minimize the space on the PCB board which makes it more suitable for projects where the power supply space plays a crucial role. The BCM device can be easily activated and deactivated using open collector input/output pin. When operated as input the voltage level on this pin should be more than 2.4 V or left unconnected. The constant voltage of 5 V can be measured on the pin when it is considered as output pin. Furthermore, the failure of the output voltage is indicated on this pin by 2 Hz square wave generated internally by DC/DC internal failure circuit. The DUT circuit was connected as it is shown in Fig. 4 (lower)

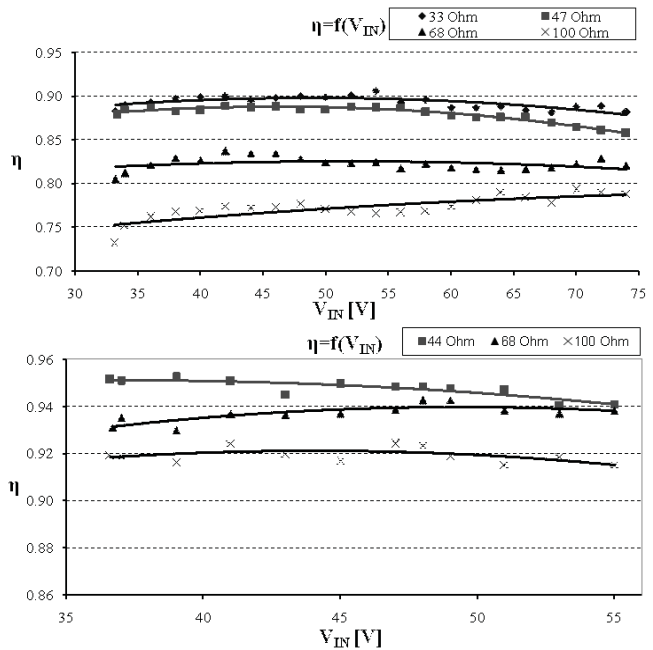


Fig. 5. Efficiency measurements for different input voltage range and resistance load – PRM-VTM (upper) and BCM (lower) configuration.

and tested with available resistance load of $44 \div 100 \Omega$. The efficiency for load of 44 Ω and nominal input voltage of 48 V was measured to be close to 95% and it is comparable to Vendor specification of such devices.

The prototype power supply unit based on two devices of B048F48T30 was designed and next used for the main power supply of 8-channels piezo drivers. The measurement stand is composed of external function generator externally synchronize using timing board, low voltage laboratory power supply of $\pm 15 V$ for supplying the pre-amplifier stages, and prototype power supply based on BCM devices for supplying power amplifiers, see Fig. 6. The piezo driver outputs were loaded with capacitance of order of 5 μF . The input signal of the power amplifiers was set to typical piezo compensation pulse of sinusoidal excitation (300 Hz, 100 mV). The timing board repetition rate was set to 2 Hz. The input voltage of the

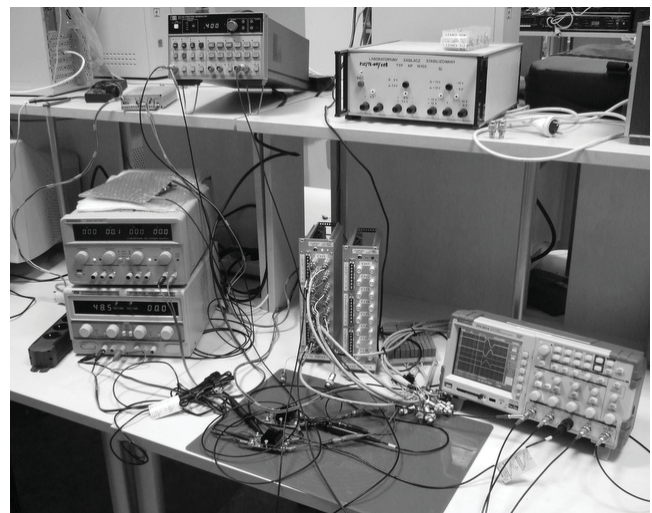


Fig. 6. The BCM power supply unit test stand used for supplying 8-channels piezo drivers.

BCM DC/DC converter was set to nominal value of 48 V using laboratory power supply, while the bipolar output voltage ± 48 V was provided to the power amplifiers. The BCM devices have been equipped with radiators in order to not activate the internal thermal protection circuits. The example measurements of the output voltage amplitude as well as output current amplitude are shown in Fig. 7.

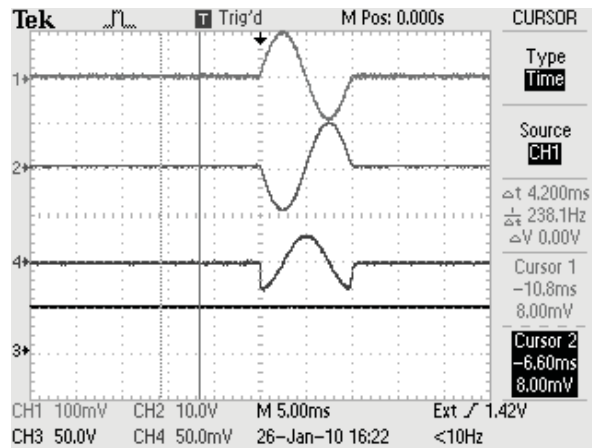


Fig. 7. The input voltage amplitude U_{im} (1), the output voltage amplitude U_{om} (2), the output current amplitude I_{om} (4) and BCM DC/DC converter output voltage (3).

IV. CONCLUSION AND FUTURE PLANS

The concept design of ATCA based piezo compensation system has been accomplished. The driving circuits together with its power supply unit – the most crucial components – has been integrated into single ATCA carrier board, see Fig. 8. The PCB board assembly and debug are scheduled for the end of 2010.

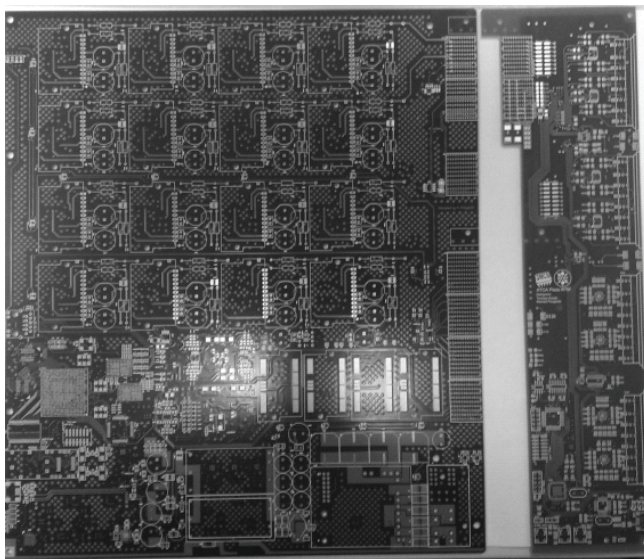


Fig. 8. The photograph of PCB board of ATCA-based piezo compensation system. On the left side Carrier board, on the right side RTM module.

ACKNOWLEDGMENT

The research leading to these results has received funding from the European Commission under the EuCARD FP7

Research Infrastructures grant agreement no. 227579 and Polish National Science Council Grant 642/N-TESLA-XFEL/09/2010/0. The authors are scholarship holders of project entitled "Innovative education".

REFERENCES

- [1] S. N. Simrock, "Lorentz Force Compensation Of Pulsed SRF Cavities," Proceedings of LINAC 2002.
- [2] G. Devanz, P. Bosland, M. Desmons, E. Jacques, M. Luong, B. Visentin, "Compensation of Lorentz Force Detuning of a TTF 9-Cell Cavity with a New Integrated Piezo Tuner," Proceedings of EPAC, Edinburgh, Scotland, 2006, pp. 378-380.
- [3] P. Sękalski, A. Napieralski, S. Simrock, "Automatic Resonant Excitation Based System for Lorentz Force Compensation for FLASH," Proceedings of EPAC, Edinburgh, Scotland, 2006, pp. 3206-3208
- [4] D. Makowski, W. Koprek, T. Jezynski, A. Piotrowski, G. Jablonski, W. Jalmuzna, and S. Simrock, "Interfaces and communication protocols in ATCA-based LLRF control systems," in Proc. Nuclear Science Symp. Med. Imag. Conf. 16th Room Temperature Semiconductor Detector Workshop, 2008.
- [5] T. Matsumoto, S. Fukuda, H. Katagiri, S. Michizono, Y. Yano, Z. Geng "Development of Digital Low-Level RF Control System Using Multi-Intermediate Frequencies," Proceedings of PAC, Albuquerque, New Mexico, USA, 2007, pp. 2110-2112.
- [6] A. Neumann, J. Knobloch, "RF Control of the Superconducting Linac for the Bessy FEL," Proceedings of EPAC, Lucerne, Switzerland, 2004, pp. 973-975
- [7] R. Cargano and others, "First Fermilab Results Of SRF Cavity Lorentz Force Detuning Compensation Using A Piezo Tuner," 13th International Workshop on RF Superconductivity Peking University, Beijing, China 2007.
- [8] S. Michizono, S. Fukuda, H. Katagiri, T. Matsumoto, T. Miura, Y. Yano, Z. Geng, "Status of The Low-Level RF System at KEK-STF," Proceedings of PAC, Albuquerque, New Mexico, USA, 2007, 2113-2115.
- [9] K. Przygoda, T. Poźniak, A. Napieralski, M. Grecki, "Piezo Control for Lorentz Force Detuned SC Cavities of DESY FLASH," Proceedings of International Particle Accelerator Conference (IPAC'10), Kyoto, Japan, 24-28 of May 2010, pp. 1452-1454
- [10] M. Grecki, A. Andryszczak, T. Poźniak, K. Przygoda, S. Sękalski, "Compensation of Lorentz Force Detuning For SC Linacs (With Piezo Tuners)," Proceedings of EPAC 2008, pp. 862-864.
- [11] T. Schilcher, "Vector Sum Control Pulsed Accelerating Fields in Lorentz Force Detuned Superconducting Cavities," PhD thesis, Universitat Hamburg, Fachbereichs Physik, Germany, 1998
- [12] K. Przygoda, W. Jalmuzna, A. Andryszczak, T. Poźniak, A. Napieralski, "FPGA Implementation of Multichannel Detuning Computation for SCLinacs," Proceedings of EPAC 2008.
- [13] W. Giergusiewicz, W. Jalmuzna, K. Poźniak, N. Ignashin, M. Grecki, D. Makowski, T. Jezynski, K. Perkuszewski, K. Czuba, S. Simrock, and R. Romaniuk, "Low latency control board for LLRF system – Simcon 3.1, Photonics Applications in Industry and Research IV, August 2005.
- [14] <http://www.radisys.com>, application notes of Radisys ATCA products.
- [15] R. S. Larsen, "Advances in Developing Next-Generation Electronics Standards for Physics", SLAC-PUB-13684, June 2009.
- [16] K. Przygoda, T. Poźniak, A. Napieralski, M. Grecki, "System For Monitoring and Compensation of Superconducting Resonant Cavities Detuning with Piezoelectric Elements," Conference of Podstawowe Problemy Energoelektroniki, Elektromechatroniki i Mechatroniki, Wisla 2009.
- [17] A. Zawada, D. Makowski, T. Jezynski, S. Simrock, A. Napieralski, "Prototype AdvancedTCA Carrier Board with Three AMC Bays," Proc. Nuclear Science Symp. Med. Imag. Conf. 16th Room Temperature Semiconductor Detector Workshop, 2008.
- [18] S. Velusamy, "LightWeight IP (lwIP) Application Examples," Application note: Embedded Processing, XAPP1026, June 15, 2009.
- [19] <https://www.vicor.com>, application notes of V•I Chips.



A. Napieralski received the M.Sc. and Ph.D. degrees from the Technical University of Łódź (TUL) in 1973 and 1977, respectively, and a D.Sc. degree in electronics from the Warsaw University of Technology (Poland) and in microelectronics from the Université de Paul Sabatié (France) in May 1989. Since 1996 he has been a Director of the Department of Microelectronics and Computer Science. In 2002 he has been elected and in 2005 reelected as the Vice-President of TUL. He is an author or co-author

of over 900 publications and editor of 18 conference proceedings and 12 scientific Journals. He supervised 44 PhD thesis; four of them received the prize of the Prime Minister of Poland. In 2008 he received the Degree of Honorary Doctor of Yaroslavl the Wise Novgorod State University (Russia).



K. Przygoda graduated from the Faculty of Electrical, Electronic, Computer and Control Engineering at Technical University of Łódź (TUL) in 2005 with MSc degree in Electronics and Telecommunications. His main areas of interests are studies of Lorentz force detuning impact on the superconducting cavities and its active compensation. He is involved in Lorentz force detuning measurements and designing the piezoelectric driving and sensing circuits and systems using FPGA devices.



T. Poźniak received Ph.D. degree in electronics from Technical University of Łódź in 1982. His research interests are power semiconductors and designing of the power converters as well as smart power devices. He is also involved in design of dedicated power amplifiers for driving the piezoelectric actuators as well as testing a prototype DC/DC converters using semiconductors fabricated using SiC technologies.



D. Makowski received Ph.D. degree in electrical engineering at the Department of Microelectronics and Computer Science Technical University of Łódź in 2006. His main areas of interests are digital electronics, embedded systems and programmable devices. He is involved in the development of xTCA standards for High Energy Physics. He is engaged in the design of distributed data acquisition and control systems based on ATCA, μ TCA and AMC standards.



T. Kozak graduated from the Faculty of Electrical, Electronic, Computer and Control Engineering at Technical University of Łódź (TUL) in 2009 with MSc degree in Electronics and Telecommunications. He continues his education as a PhD student at TUL in fields of control and data acquisition systems for High Energy Physics experiments and gamma and neutron radiation influence on electronics systems.



M. Grecki received Ph.D. degrees in electronics from Department of Microelectronics and Computer Science Technical University of Łódź in 1995. The main area of his interests are gamma and neutron radiation influence on electronics systems. He is also involved in the development and design of the LLRF control systems dedicated for the FLASH and X-FEL linear accelerators.