Fault Modeling and Analysis of Short Defects in CMOS Based Reversible Circuits

Alexandru Amaricai, and Oana Boncalo

***Abstract*—This paper presents a SPICE based analysis of reversible circuits affected by the short defects: the gate oxide defect and the source-drain defect. The simulations are performed using realistic transistor models (the BSIM4 model) and take into account the resistive nature of the gate oxide and the source drain shorts. We aim at determining dependence between the short's resistance and the output voltage. Furthermore, we analyze the timing characteristics of reversible circuits affected by such faults. The goal is to develop logic and delay fault models for CMOS based reversible gates. This way, Boolean test strategies and logic level fault tolerant mechanisms and strategies can be devised for reversible circuits.**

***Index Terms*—Reversible circuits, fault modeling, testing, short**

I. Introduction

ONE of the most important factors in today's digital electronic circuits is represented by the power consumptions. As the transistor's size decreases and the number of transistor numbers in an integrated circuit increases, the power consumption becomes more and more prohibitive. A major key factor in the energy dissipation of electronic devices is represented by the irreversible nature of the computation. Thus, for every lost bit of information during a logic computation (such as logic NAND between two input variables) an amount of heat is generated [6][7][8][12]. One possible way of reducing power consumption is by employing reversible circuits. Reversible computing performs logic operation without information loss. Furthermore, reversible computing is used in quantum computing (almost all quantum operations are reversible), but also in optical computing, DNA computing and nanoelectronics [8][12][21].

Significant developments have been brought to reversible computing in the last decade. Logic level designs for a wide range of combinational circuits (such as ALU's) have been proposed. Logic synthesis algorithms, methodologies and tools have been developed [11][12][21]. Furthermore, sequential reversible circuits have been also proposed [5][15]. More important, physical reversible combinational devices have been implemented using CMOS transmission gates (such as adders, multipliers, filters, FFT circuits, etc) [6][13] [17][20]. Therefore, a wide range of design methodologies at different abstraction levels have been developed for reversible circuits.

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A major component issue in the marketing of today's integrated circuits is represented by testing. As current CMOS technology scales down, the defect rate in present chips is increasing. As reversible circuits can be implemented using CMOS technology, the high defect rate will affect them to. Therefore, in order to develop commercial reversible devices, test algorithms and test strategies (such as design for testability, built-in-self-test, etc) have to be devised. Furthermore, fault tolerant algorithms and mechanisms have to be implemented in order to manage the increased defect rate. Therefore, different abstraction layers (electric, logic, RTL, architectural) fault models are required. As reversible circuits using CMOS transmission gates do not present supply or ground lines, classic fault models such stuck-at-0 or stuck-at-1 cannot be used. Hence, fault models for these devices must be devised in order to develop testing strategies and fault tolerant algorithms and mechanisms.

In this paper, we present a SPICE based analysis of the NMOS and PMOS short defects (source-drain, gate-drain and gate-source resistive shorts) which affect reversible circuits implemented with transmission gates. We analyze the relationship between the output voltage and the short resistance. Furthermore, we determine the effect of the short defect on the timing characteristics of the reversible gates.

The paper is organized as follows: Section II is dedicated to the CMOS transmission gates based reversible circuits, Section III is dedicated to the source-drain and gate oxide shorts and their electrical modeling, while in Section IV simulation results are presented; concluding remarks are presented in the last section.

II. CMOS Based Reversible Gates

Reversible circuits have been implemented using CMOS transmission gates by De Vos et al [6][13][17][20]. These circuits use the following reversible gates (which form a universal reversible gate set): Not gate, Controlled-Not gate, Toffoli gate (Controlled-Controlled-Not) and the Fredkin gate (Controlled-Swap). Fig. 1, 2 and 3 presents the structure of these reversible gates.

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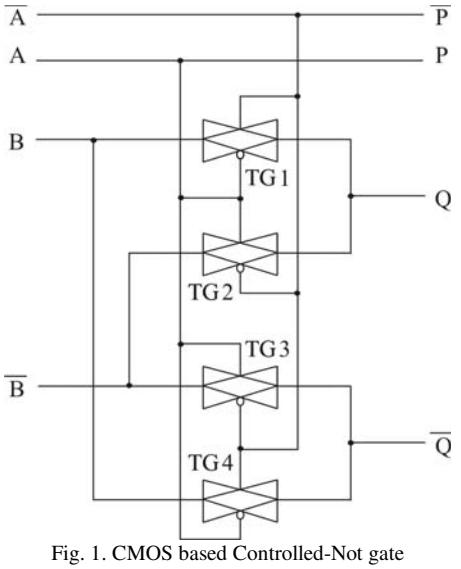


Fig. 1. CMOS based Controlled-Not gate

The classical CMOS circuits (such as Not, Nand or Nor gates) use the so called restoring logic for their operation. Their outputs are "connected" (depending on which transistor is conducting and which is blocked) either to the ground line (when the output is '0' logic), either to the Vdd line (when the output is '1' logic). The reversible gates are implemented using a dual logic approach [6][13]: for each input/output logic variable, two signals are used: the one corresponding to the variable and its negated form. Therefore, the circuits' outputs are powered only by their inputs. Therefore, there is no need for power or ground bars in reversible devices. The power required for driving the inputs comes from [6][13]:

- ideal voltage sources
- input memory registers
- standard CMOS circuits.

These circuits are well suited for adiabatic switching. In many cases, triangular signals are used as their input. In Fig. 4 the input and the output signals of a reversible adder circuit is depicted (as presented by de Vos et al [6]).

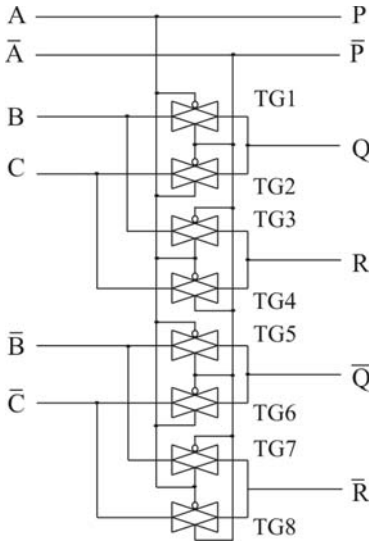


Fig. 2. CMOS based Fredkin gate (Controlled-Swap)

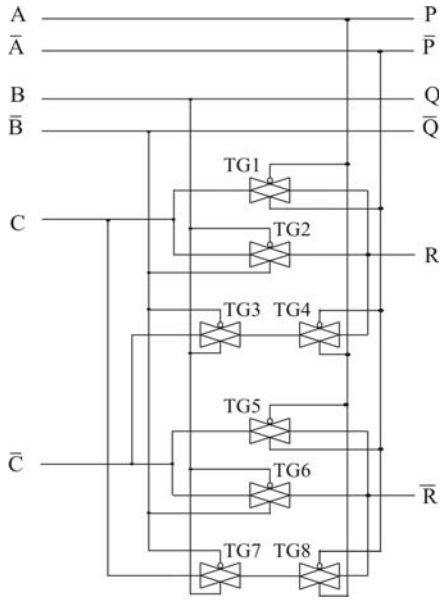


Fig. 3. CMOS based Controlled-Controlled-Not (Toffoli) gate

Regarding the cost of the reversible gates, the one bit Not gate requires no transistors, the two bit Controlled-Not requires 4 transmission gates (8 MOS transistors), while the three bit Toffoli and Fredkin gates require 8 transmission gates (16 transistors) [6][13][17][20]. Based on these gates, several combinational reversible circuits have been implemented, such as adders, multipliers, Fourier transform circuits or discrete linear filters. As these circuits are not connected to the ground and power lines, classical fault models such as stuck-at-0 or stuck-at-1 cannot be applied in these cases. Therefore, new fault models have to be devised for reversible gates.

III. CMOS Short Defects

The most common defects which are found in today's integrated circuits are shorts and opens. In the case of the MOS transistor, nine defects can affect it – Fig. 5 [16]:

- Gate-source short
- Gate-drain short
- Gate-channel pinhole
- Source-drain short
- Drain-substrate short
- Source-substrate short
- Open gate
- Open source
- Open drain

The most prevalent types of short defects are the gate oxide shorts (Fig. 6) and the source-drain shorts (Fig. 5). Regarding the source-drain short, the result is a transistor that always conducts [16][19].

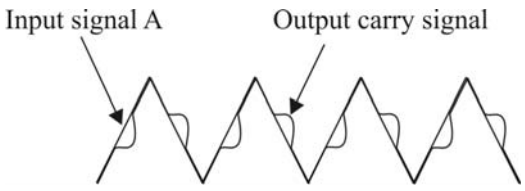


Fig. 4. Input and output signals in a reversible adder [6]

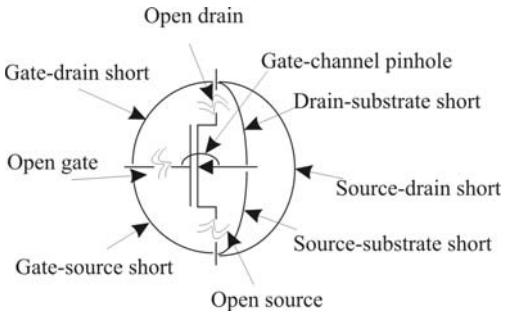
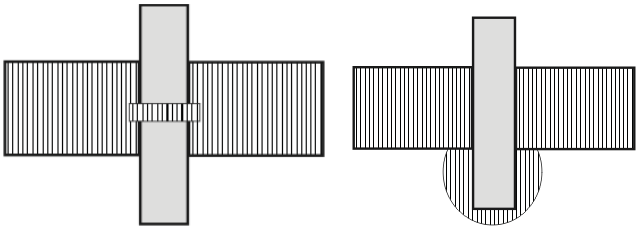


Fig. 4. MOS transistor defects [16]

This type of defects are caused by a missing section of the gate over the transistor channel (Fig.5.a), by extra diffusion area around the gate between the source and drain (Fig. 5.b) or by punchtrough of the transistor channel which leads to a permanently conducting transistor (due to electrostatic discharge or a high drain voltage) [14][16][19]. The source drain short defect is modeled by a resistor. Usually, the value of the resistor is between 50 ohms and 5000 ohms [16]. A similar effect is also obtained in the case of an intra-gate bridge which affects the CMOS transmission gate [4].

The gate oxide defects (gate-source and drain-source shorts) are the most common in some CMOS processes [9][10][13][14][19]. It consists of an electrical connection between the gate (which is usually made of n-type polysilicon) and the source, drain or the channel (p-well or n-well) – Fig 6. Theses defects do appear in either the fabrication process, or during the exploitation of the integrated circuit. They usually are the result of electrostatic discharge or electrical overstress [18]. In these cases, the effect is similar to a resistive short between the gate and the source or drain.

Regarding the electrical modeling, in this paper we will consider the polysilicon layer which composes the gate fabricated using n-doped silicon, as in [9][10][18]. Therefore, in the case of NMOS transistor, a gate-source and a gate-drain defect is modeled as a simple resistor – Fig 7.a. In the case of the PMOS transistor, a pn junction appears at the gate oxide short. Therefore, a diode in series with a resistor is used to model for a gate-source or a gate-drain short defect – Fig 7.b. In both cases, the value of the resistance depends on a wide



a) b)

Fig. 5. Source-drain shorts a) Due to missing gate area
b) Extra diffusion area

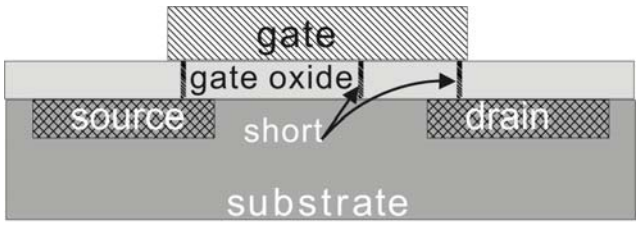
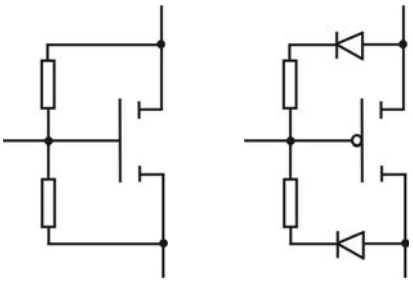


Fig. 6. MOS gate oxide shorts



a) b)

Fig. 7. Electrical modeling of gate-source and gate-drain shorts for NMOS (a) and PMOS(b)

range of factors: defect size, oxide thickness, doping densities, and electrical causes and conditions of the breakdown. Usually, the value of the short resistance is considered to be between 100 ohms and 5000 ohms [9][10][16].

IV. Simulation Results

We perform an analysis of the behavior of a defect Controlled-Not gate. The transistor model used in simulations is a BSIM4 50 nm model described in [2]. The circuit under test used in the analysis is depicted in Fig. 8. The main reason is represented by the fact that both inputs are connected to the outputs from other reversible circuits, and not outputs of an ideal voltage sources. Transmission gate 1 from the third Controlled-Not gate is affected by defects. A 1 volt voltage represents logic '1', while a logic '0' is represented by the ground level. The resistance value is between 50 and 5000 ohms. The considered load capacitance is 50 fempto-farads.

A. Logic Fault Modeling

In order to determine the logical behavior of the reversible gates affected by short defects a static analysis has been performed. The gate oxide defects have been analyzed in [1], while the source-drain defects have been analyzed in [3].
The following cases do appear:

1. *NMOS Gate-Source Defect* – In this case a bridging between the C and /D inputs do appear. Simulations show that a faulty transmission gate1 is detected when the C and D inputs have the same logic value. When the value of the short resistance is small enough the two pair of outputs (P and /P on one hand and D and /D) have similar voltage values, thus similar logic behavior. Therefore, the circuit does not present the dual logic behavior anymore. The results are plotted in Fig 9, which presents the dependence of the voltage of C, /D, P and /P for logic '0' inputs at C and D. Therefore, in order to detect this kind of fault, the two inputs must have the same logic value.

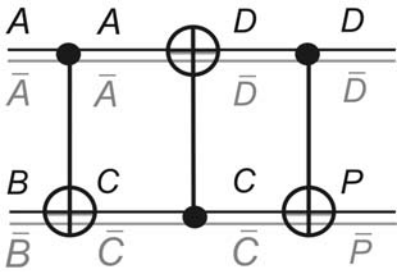


Fig. 8. Circuit under test – the transmission gate 1 of third CNOT gate is affected by defects

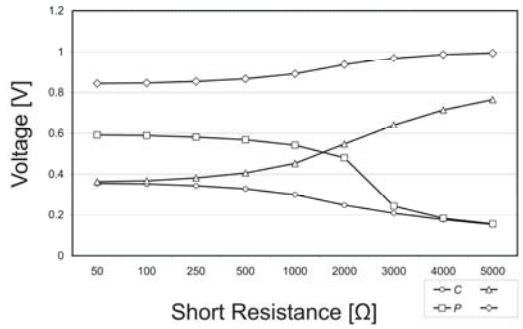


Fig. 9. Dependence between voltage and short resistance for a NMOS gate-source defect

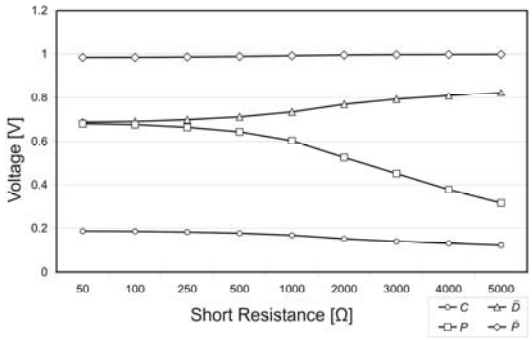


Fig. 10. Dependence between voltage and short resistance for a NMOS gate-drain defect

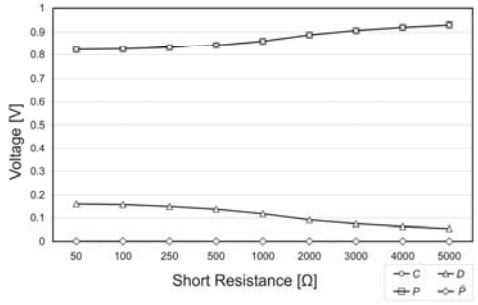


Fig. 11. Dependence between voltage and short resistance for a PMOS gate-source defect

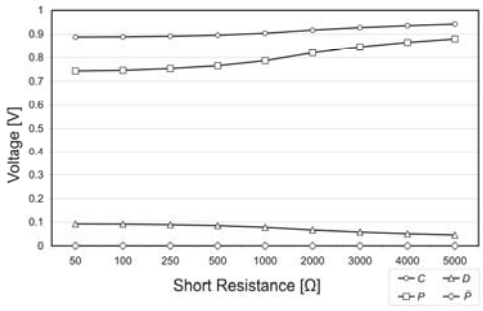


Fig. 12. Dependence between voltage and short resistance for a PMOS gate-drain defect

2. *NMOS Gate-Drain Defect* – This defect leads to a bridging between the control input /D and the data output P. Fig. 10 presents the dependence of the voltage of C, /D, P and /P and the short resistance values, when C and D are logic '0'. The results show that this type of defect which appears at transmission gate 1 can be detected when the outputs P and /D have different logic values. When the short resistance is small, the output P has the same logic value as the input/output /D. When P and D have different logic values, this defect cannot be detected by Boolean testing.
3. *PMOS Gate-Source Defect* – This defect result in a bridging between the input lines /D and C, when the diode is forward biased. However, the diode's internal resistance is added to the short resistance. Therefore, the effect of this defect is smaller compared to the NMOS transistor [9]. The simulation results are presented in Fig 11. This fault manifests when the C input is logic '1' and D input is logic '0'. As presented in Fig 11, the logic values of the outputs are correct. This is due to the diode that appears at the short location. Thus, this defect cannot be tested using Boolean tests.
4. *PMOS Gate-Source Defect* – A bridging between the output lines /D and P does appear when the diode is forward biased. As in the previous case, the effect of this fault is much smaller compared to the NMOS transistor. The results are plotted in Fig 12. The fault can be detected when the D output is 0 and P output is 1. As in the previous case, this defect cannot be detected using Boolean tests.
5. *Source-Drain Short Defect* – A bridge does appear between the C input and the P output. A source-drain short defect at transmission gate 1 can be detected when the transmission gate 2 is activated, while the other one is blocked. This is valid for a logic "1" D input. The results are plotted in Fig 13. The logic behavior of a gate affected by this type of defect is characterized by a link between one input and one output.

B. Delay Fault Modeling

In order to determine the delay properties of the faulty gates, we have used triangular signals (t_{rise}=20 ns, t_{fall}=20 ns, while V_{max}=1V and V_{min}=0V) as inputs to the circuit in Fig 8. This type of signal has also been used as input for reversible circuits by de Vos et al in their physical implementations in CMOS technology. The considered short resistance used is 5000 ohms. The goal is to determine timing issues of reversible gates affected by faults which cannot be detected by simple Boolean testing. Simulation results are presented in Fig. 14.

Simulations show that at least one timing parameter is affected by a high short resistance values. In the case of the source-drain short (Fig 14-c), the low to high transition delay

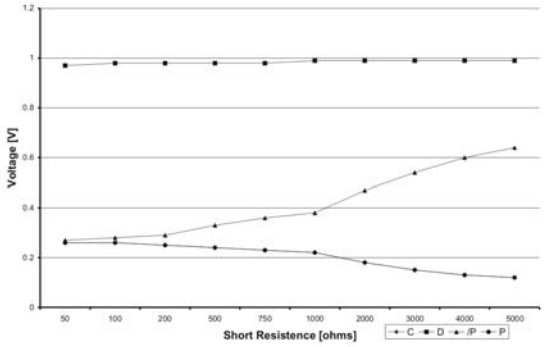
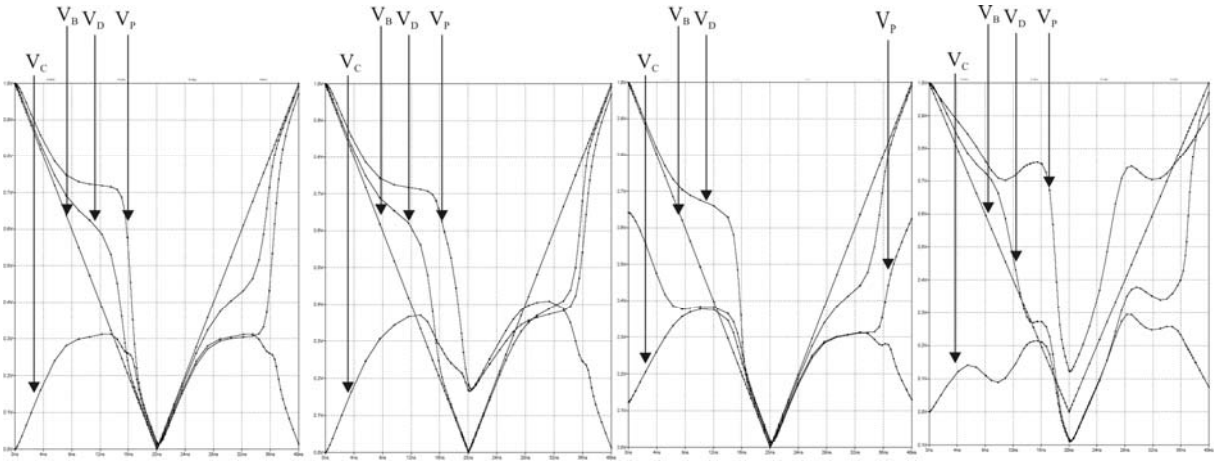


Fig. 13. Dependence between voltage and short resistance for a source-drain defect



a) b) c) d)

Fig. 14. Transient analysis a) Fault free b) NMOS Source-Gate Short c) Source-Drain Short d) PMOS Source-Gate Short

is increased for a defect gate, while the high to low transition delay is decreased.

V. CONCLUSION

This paper presents a SPICE based analysis of reversible gates affected by short defects: gate oxide shorts and source-drain shorts. Two types of analysis have been performed: a static analysis, which aimed at determining the logic behavior of faulty reversible gates, and a transient analysis, which aimed at determining timing issues related to the faulty gates.

The results show that for the NMOS gate oxide shorts and for the source-drain shorts, low values of the short resistance do affect the logic behavior of the CMOS based reversible circuits. In these cases, Boolean testing can be applied in order to detect these faults. In these cases, the reversible circuits do not present the dual logic behavior required for these circuits o operate.

The PMOS gate defects and when the short resistance value is high, Boolean testing cannot be applied in order to detect faults. Gates affected by these types of faults have different output voltage values or different timing parameters. Thus, output voltage measurement or delay measurements can be used to detect these faults.

Regarding future work, we will focus the propagation mechanisms of these types of defects. Thus, testing algorithms and methodologies for short defects that affect reversible circuits can be devised. Furthermore, we aim to analyze the open defects in a similar manner.

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