# Methodology for the Digital Calibration of Analog Circuits and Systems Using Sub-binary Radix DACs

Marc Pastre and Maher Kayal
E-Lab
EPFL
CH-1015 Lausanne, Switzerland

***Abstract*—This paper presents a methodology for digitally calibrating analog circuits and systems. Based on the detection of an imperfection by a simple comparator, a successive approximations algorithm tunes a compensation current. The latter is generated by a sub-binary radix M/2$^+$M DAC, which has the advantage of allowing reaching arbitrarily high resolutions at the cost of extremely small area. The methodology proposed allows the removal of any type of imperfections, at the expense of two shift registers, a few logical gates and a DAC which is smaller than the shift register.**

***Index Terms*—Calibration, sub-binary DACs, M/2$^+$M, offset compensation, deep sub-micron, variability.**

## I. Introduction

The evolution of integrated circuit manufacturing technologies renders even basic analog systems difficult to design today. With the size reduction, the intrinsic precision of the components degrades. In parallel, the supply voltage decreases, limiting the topologies which can be used. Many modern technologies are specifically suited for pure digital circuits, and some analog devices, like capacitors, are not available. In these conditions, analog design is a challenge even for experienced designers. To relieve the extreme design constraints in analog circuits, digital calibration becomes a must. It allows a low-precision component to be used in high-performance systems. If the calibration is repeated, it can even cancel the effect of temperature drift and ageing.

The digital calibration is compatible with the evolution of fabrication technologies, which ever more facilitates the integration of digital solutions at the cost of a dramatic reduction of analog performances. Thanks to the reduction of the size of digital devices, even complex digital calibration solutions can be integrated and become a viable alternative to intrinsically precise analog designs. Digital calibration allows realizing high-performance analog systems with modern technologies. This enables pure analog designs to be implemented even in fully digital processes. In existing mixed-signal designs, the full system realization also becomes possible with technologies providing higher integration density. Finally, because circuit performances rely on digital calibration, retargeting is simplified. The digital blocks can be synthesized automatically, whereas only a limited design effort is invested in the analog circuit.

The methodology presented in this paper is versatile. It can be applied at circuit or system level, for analog circuits, but also mixed-mode circuits like sensor interfaces [1][2][3], and even purely digital systems like memories [4][5][6].

## II. Digital Compensation of Analog Circuits

Figure 1 presents a synoptic view of a digitally calibrated analog system. The digital calibration shown in grey aims cancelling an imperfection of the analog system. As explained above, this is a viable alternative to building an intrinsically precise analog system which reaches high specifications on its own, without requiring calibration.

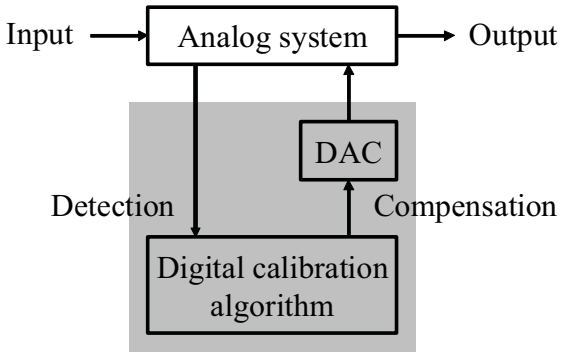


Figure 1. Digital calibration of an analog system.

To allow the digital compensation of an imperfection in an analog circuit by the injection of a compensation current, two nodes must be identified in the analog system: a *detection node* and a *compensation node*. Furthermore, a *detection configuration* of the compensated analog circuit must be found. The observation of the detection node allows determining whether the imperfection to be corrected is lower or higher than the error-free nominal value to be reached by calibration. For example, the offset of an operational amplifier is positive or negative around the nominal value 0. Based on the information gathered in the detection node, an adequate decision is taken to compensate the imperfection by increasing it if it is lower than expected or decreasing it if it is higher than the nominal value.

### A. Detection Configuration

The detection configuration is the condition in which the circuit imperfection can be observed in the detection node. In some cases, this is possible during normal circuit operation,

without modifying the circuit topology and interrupting signal processing. But in many cases, a different circuit configuration is necessary to measure the imperfection in the detection node. Usually, this is due to the low level of signal at the detection node during normal operation. Figures 2 and 3 present the typical example of the offset cancellation of an operational amplifier.

During normal operation in closed-loop (Figure 2), the offset of the amplifier can be sensed directly between its two inputs. The detection signal δ is:

$$\delta = V_{in+} - V_{in-} = -V_O \tag{1}$$

The detection signal level is problematic though. Indeed, at the end of the calibration procedure, the residual offset of the amplifier is:

$$V_{O;compensated} = V_{OC} \tag{2}$$

This imposes that the comparator used to determine the offset sign has an offset lower or equal to the expected residual offset of the amplifier after calibration.

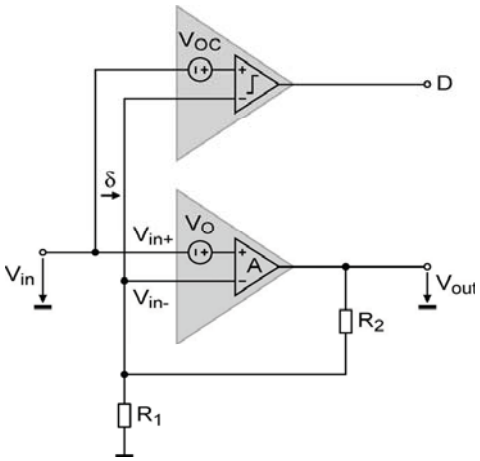


Figure 2. Closed-loop offset cancellation.

To overcome this severe limitation, two options can be considered. The first one is to compensate the offset of the comparator (in an open-loop configuration) before using it to correct the offset of the amplifier in closed-loop. The second possibility is to measure the offset of the amplifier using the open-loop configuration of Figure 3.

In this topology, the detection signal is:

$$\delta = AV_O \tag{3}$$

where A is the open-loop gain of the operational amplifier. This second configuration presents the advantage of having a detection signal being several orders of magnitude higher than the closed-loop one. As a consequence, the residual offset after calibration becomes:

$$V_{O;compensated} = -\frac{V_{OC}}{A} \tag{4}$$

The comparator offset is no more critical and thus doesn't need to be calibrated preliminarily.

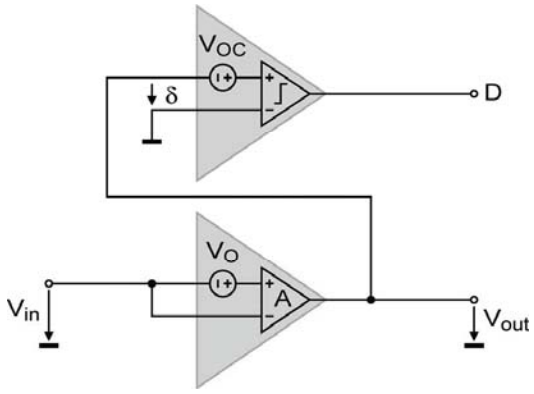


Figure 3. Open-loop offset cancellation.

The disadvantage of the open-loop configuration is the fact that it requires to remove the amplifier from its normal operation mode. In some applications, this is acceptable. If continuous signal processing is required, a strategy with two amplifiers being alternatively one calibrated and the other operating normally (ping-pong) can be implemented [7].

### *B. Detection Node*

In the selected detection configuration, there should be a detection node identified where the imperfection to be compensated can be sensed appropriately. In particular, the signal level should be sufficiently high, and the signal measured should be a function of the imperfection alone. The imperfection can be sensed in current or voltage mode, single ended or differentially. If single-ended mode voltage detection is chosen and if the offset of the comparator is not critical, an implementation as simple as a digital inverter can be considered. Figure 4 shows how the circuit of Figure 3 can be simplified.

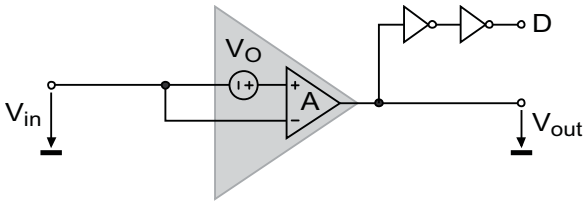


Figure 4. Digital calibration of an analog system.

### *C. Compensation Node*

The correction is done by injecting a compensation current in an appropriate node of the analog circuit. The compensation

node is chosen for its property to convert the injected current into a reduction/increase of the imperfection. In the ideal case, no other parameter should be affected by the compensation current. In practice, the correction node is chosen for the high correlation between the injected current and the imperfection, and the low correlation between the compensation current and any other parameter. Figure 5 shows the implementation of a differential current compensation of a Miller operational amplifier.

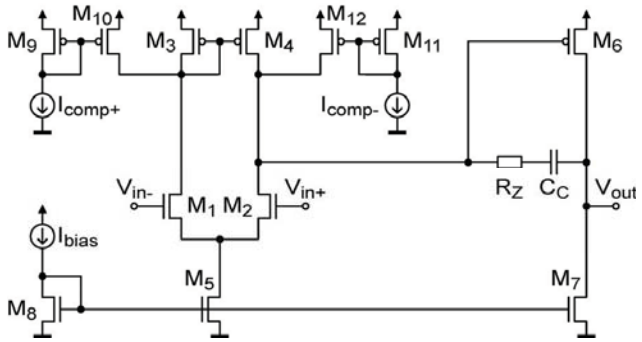


Figure 5. Differential compensation of a Miller operational amplifier.

In this circuit, the compensation current mirrors use PMOS transistors and the current is injected in the same direction differentially. This allows the direct connection of an M/2+M ladder to the compensation current inputs, transistors $M_9$ and $M_{11}$ being the current collectors. Alternative compensation circuits could inject the compensation current unilaterally.

For the choice of the compensation node, attention must be paid to not degrading circuit performance. This implies that the current mirrors added (transistors $M_{10}$ and $M_{12}$ in Figure 5) don't add significant parasitic capacitances to the compensation nodes, and that their output impedance is higher than the impedance in the compensation nodes.

The dimensioning of the compensation current mirrors in the case of the Miller operational amplifier is done as follows:

1. The maximum compensation current is determined.
2. The transistor length L is determined in order to have a sufficiently low channel conductance gds that does not affect much the impedance of the compensation node. The length must also be sufficient to limit the effect of voltage variations in the compensation node on the compensation current that is injected.
3. The transistor width W is calculated, considering that the output transistors of the current mirrors must remain in saturation. The width must be large enough to keep the saturation voltage below the voltage in the compensation node.

## III. Successive Approximations

The successive approximations algorithm performs a search through the possible values of the compensation currents. It performs dichotomy at each step, by determining whether the tested bit generates a compensation value too high or not. The algorithm starts by testing the most significant bit (MSB), and goes down towards the least significant bit (LSB). Figure 6 presents a pseudo-code description of the algorithm, with $d_i$ ($i \in [1, n]$) being the digital input word of the n-bits DAC, and $C_{out}$ the output of the comparator.

```
reset all di = 0
for i = n downto 1
   set di = 1
   if Cout > 0
      reset di = 0
   end if
end for
```

Figure 6. Successive approximations algorithm.

First, all bits are cleared (D = 0). Then, the bits are tested successively in a loop, starting with the MSB and going down to the LSB. For each bit, the output value of the comparator $C_{out}$ is examined when the bit is set. If the value is negative, this signifies that the remaining imperfection is negative and that the DAC value has still to be increased. For this reason, the bit is kept. If on the contrary $C_{out}$ is positive, the currently tested code is too high and the tested bit is reset. The algorithm then performs the same test with the next less significant bit, until reaching the LSB.

### A. Working Condition

For the successive approximations algorithm to work properly, the following condition has to be met:

$$b_i \le b_1 + \sum_{j=1}^{i-1} b_j \ , \ i \in [2, n] \tag{5}$$

The working condition guarantees that the sum of the less significant bits of any bit $b_i$ in the DAC is not inferior by more than one LSB to the bit itself ($b_i$). This ensures that if a bit $b_i$ is rejected during a given step of the successive approximations algorithm, the remaining steps using only less significant bits cover the complete range of values up to the value just rejected.

## IV. Sub-Binary Radix DACs

Using a binary-radix DAC with a successive approximations algorithm exploits the limit of the working condition. Indeed, for a binary-radix DAC, one can write:

$$b_i = b_1 + \sum_{j=1}^{i-1} b_j \ , \ i \in [2, n] \tag{6}$$

Binary-radix DACs are difficult to design unless the number of bits is small, because the weight of each bit needs to be precisely set to avoid missing codes and redundancies. For this reason, they usually occupy an important circuit area.

The working condition of the successive approximations algorithm does not impose precise bit weights. Whereas missing codes are not allowed, redundancies are not

problematic. This can be turned into an advantage, because it allows the use of imprecise converters. By voluntarily introducing redundancies, the risk of missing codes is reduced and the sub-binary converters can be designed using less effort and area without degrading the performance of the algorithm.

Figure 7 presents the input/output characteristics of a 4-bits radix-1.5 DAC. One can see that it has a resolution of 3 bits (the LSB is 1 on a full scale of 8), and that it presents several redundancies, in particular for the codes where the MSBs change values.

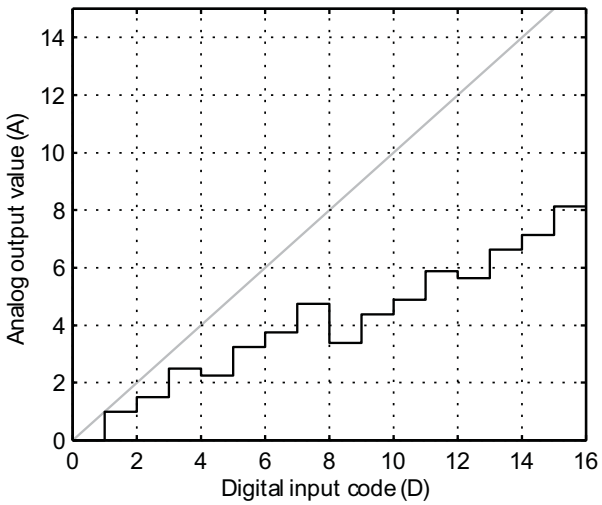


Figure 7. Input/output characteristics of a 4-birs radix-1.5 DAC.

It is noteworthy that the working condition of the successive approximations algorithm is achieved equally in each stage. This means that adding an extra bit does not imply an increase in circuit area for matching purpose. Each stage of the converter has a given area fixed by component mismatches, and adding an extra bit simply costs the area corresponding to one more stage.

*Sub-binary converters should thus systematically be used with successive approximations algorithms*. There is no reason for preferring a conventional radix-2 converter.

### A. Radix choice

To limit the number of stages in the DAC, the radix should be chosen as high as possible (close to 2). However, the need to guarantee that the DAC will have no missing code, the maximum radix depends on component mismatch. Figure 8 presents the maximum radix R allowed for not violating the working condition of the successive approximations algorithm as a function of the worst-case component mismatch δ.

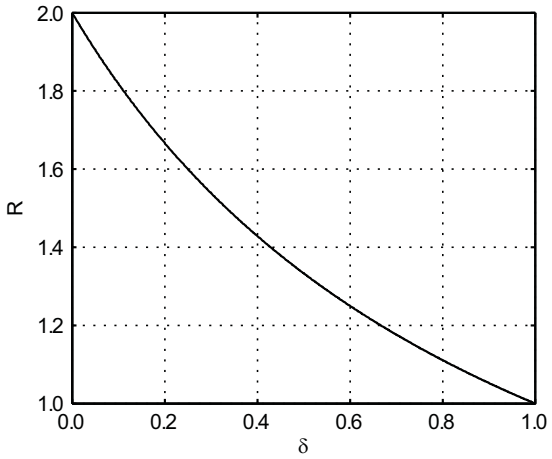


Figure 8. Maximum radix allowed for a given component mismatch.

It can be seen that for perfect components (δ = 0), a radix-2 converter can be implemented. When the mismatch is 100%, the only choice is a thermometric scale, where each bit has the same weight. Typical values of mismatches lie around 10%, which corresponds to a radix value of 1.8.

### B. Resolution

The full scale current of the DAC is chosen to cover the whole range of imperfection to be cancelled ($Imp_{uncompensated;max}$).

Then, the necessary resolution of the sub-binary DAC can be expressed as the ratio between the maximum magnitude of the imperfection to be compensated and the worst-case residual imperfection expected after calibration ($Imp_{compensated;max}$):

$$Resolution = \frac{FullScale}{LSB} = \frac{Imp_{uncompensated;\max}}{Imp_{compensated;\max}} \tag{7}$$

For a n-bits sub-binary radix-R DAC, the full scale is equal to:

$$FullScale = b_1 \frac{R^n - 1}{R - 1} \tag{8}$$

This corresponds to a radix-2 equivalent resolution of:

$$Resolution = \log_2\left(\frac{R^n - 1}{R - 1} + 1\right) \tag{9}$$

In practice, for radices close to 2, only a few additional bits are needed to reach the equivalent resolution of a radix-2 converter. A simple approximation gives:

$$N_{extra-bits} = N_{bits}\left(1 - \frac{R}{2}\right) \tag{10}$$

where $N_{bits}$ is the number of bits of the radix-2 implementation. This additional cost is negligible in terms of circuit area, because every stage in a sub-binary DAC occupies the same area and that the area per stage doesn't increase with resolution. This is not the case for binary radix DACs.

## V. Sub-Binary R/2$^+$R DACs

Sub-binary radix DACs can be implemented advantageously in R/2R-like structures. Figure 9 shows such a ladder where the resistors in the vertical branches have a value xR, except the terminator which has a $x_T$R value.

When $x = x_T = 2$, the ladder is the well-known R/2R.

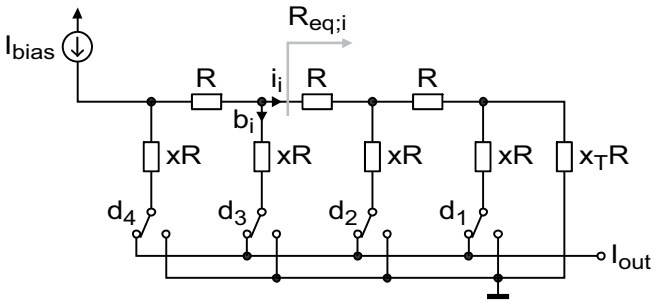


Figure 9. R/xR ladder.

For a R/2R ladder, the equivalent resistor $R_{eq;i}$ in each stage is equal to 2R. This implies that the current division in each branch is done equally, i.e. $b_i = i_i$. But since $i_i$ is the sum of the least significant bits plus one LSB, equation (6) holds for this ladder. The consequence of this is that even the slightest mismatch on the resistor values translates into a missing code.

To avoid this situation, the ladder is made sub-binary by choosing a value of $x > 2$. The equivalent resistor $R_{eq;i}$ then becomes lower than xR, and the current division makes the sum of the remaining bits higher than the bit current:

$$b_i < i_i = b_1 + \sum_{j=1}^{i-1} b_j \tag{11}$$

This is the favorable situation with respect to the working condition of the successive approximations algorithm (equation 5). The ladder now tolerates a resistor mismatch and the DAC will have no missing code if the radix, or equivalently the xR value, is chosen according to Figure 8.

## VI. Sub-Binary M/2$^+$M DACs

The realization of sub-binary radix DACs with resistors is not optimal in terms of circuit area. An implementation based on transistors [8] is much more compact.

In the resistive ladder, each elementary resistor is replaced by a MOS transistor of fixed dimensions W over L (equal for all transistors). The gate voltages $V_G$ are the same for all transistors in the ladder. At these conditions, the transistor-based circuit divides the current linearly as resistors [9][10].

Figure 10 shows the transistor translation (M/3M) of a R/3R ladder.

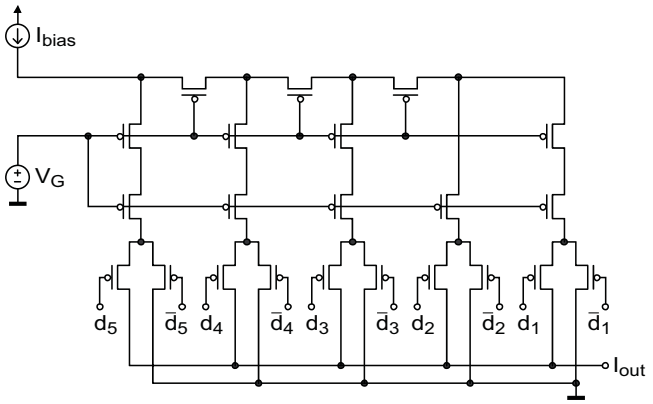


Figure 10. M/3M ladder.

In each stage horizontally, there is one single transistor implementing an equivalent R transistor. In each vertical branch, there are 3 transistors in series which implement an equivalent 3R resistor. In each stage, the two bottom-most transistors also have the role of switching the current either to the output or to ground. To achieve that, one transistor is biased with a gate voltage equal to $V_G$, which makes it behave like the third 1R resistor needed in each vertical branch, whereas the other transistor in parallel is disabled by applying a gate voltage equal to $V_{dd}$. In the network of Figure 10, an advantageous choice is to set $V_G = V_{ss}$, because this allows driving the $d_i$ digital control signals directly with logic.

The penultimate (2) stage in the network is designed to generate locally a sub-binary current division for the LSB. Its implementation is kept as simple as possible so that the regular structure of the network is not broken.

Other radices can also be implemented with M/2$^+$M structures. Figure 11 shows an implementation of a M/2.5M ladder.

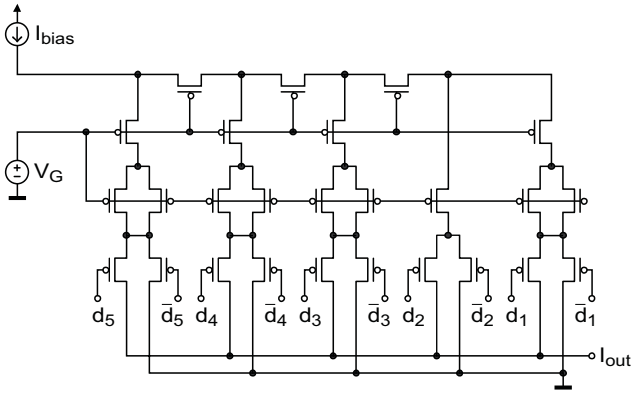


Figure 11. M/2.5M ladder.

In this circuit, the middle transistor in each vertical branch is put in parallel with a second one. The equivalent vertical resistance thus indeed becomes 2.5R.

The M/2.5M ladder exhibits a radix slightly higher than a M/3M ladder. This has the advantage of needing fewer additional bits, but imposes to have better matched transistors. Table I summarizes the characteristics of both networks.

TABLE I. M/2+M LADDER CHARACTERISTICS

| Parameter | Value | |
|---|---|---|
| | *M/2.5M* | *M/3M* |
| Radix | 1.86 | 1.77 |
| Maximum allowed mismatch | 7.3% | 13% |

### A. Current collectors

The output current from the M/2$^+$M ladder can be collected by current mirrors. Figure 12 shows a differential output circuit collecting both currents from the current division network. The two outputs can be used to drive the compensation nodes, as shown in Figure 5.

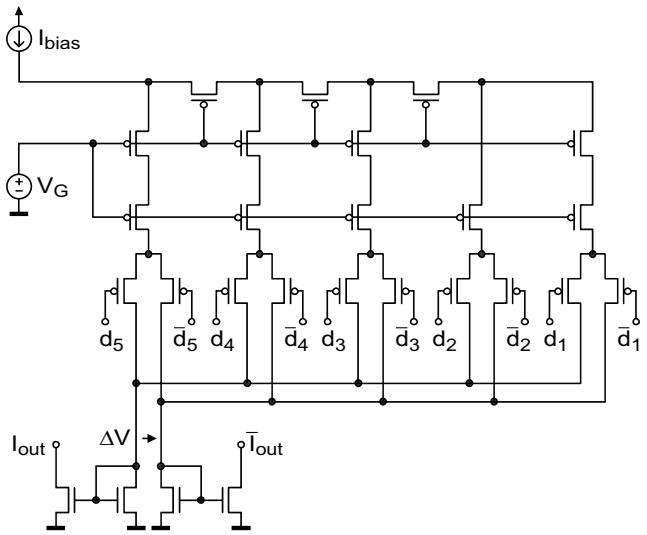


Figure 12. M/3M ladder with current collectors.

## VII. CIRCUIT LAYOUT

The M/2$^+$M ladders are regular structures, whose layout can be done as arrays. Since the allowed transistor mismatch is around 10% and because an increased number of stages doesn't require better matching, the transistor dimensions (W and L) can be kept small. Figure 13 shows a micrograph of a 17 stages M/3M ladder, with two current mirrors as an output stage as in Figure 12, and a digital register used for storing the ADC input code. It can be observed that the DAC is smaller than the digital register, and that the output stage is also a compact structure.

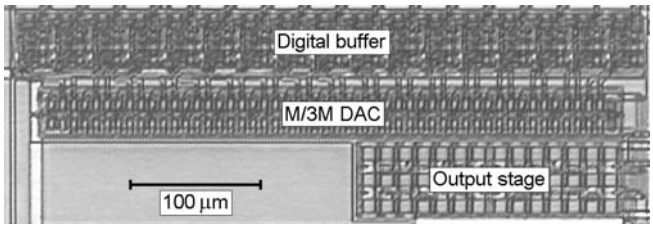


Figure 13. 17-stages M/3M ladder, with current collectors and input buffer.

## VIII. CONCLUSION

The methodology presented in this paper allows the systematic and versatile compensation of imperfections in analog circuits using simple digital circuits and an area-efficient sub-binary DAC implementation. At the cost of a circuit area equivalent to only a few digital registers (including the DAC and its output stage), an imperfection can be corrected with an arbitrarily high resolution. This enables high-performance analog design even in deep sub-micron technologies, where process variability is problematic and the degrees of freedom for analog design are severely restricted.

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