

Interconnections Coupling through Substrate for Frequencies up to 100GHz

Vasileios Gerakis, and Alkis Hatzopoulos

Abstract—This work presents a study on the substrate noise coupling between two interconnects. A highly, a lightly and a uniformly doped substrate, approximating most modern technologies, are described. The three different doping profiles are simulated for various interconnect distances and different metal layers assuming a 65 nm bulk CMOS technology. A proper data analysis methodology is presented, including z and s parameters extraction and de-embedding procedure.

Index Terms—Substrate noise; Interconnect coupling; Substrate doping; s parameters; z parameters.

I. INTRODUCTION

SUBSTRATE noise issues have become more concerning as the CMOS technology increases its scaling. The need of studying them up to 100 GHz has become really important due to the fact that practical applications like, for example, automotive radar or backhaul radio links are implemented at these extremely high frequencies [1].

Although the substrate coupling effect has been studied, less attention has been given to the effect of the process doping profile to the noise levels. Moreover, simulation data from some commercial simulators need to be de-embedded due to the auxiliary connecting structures required for the simulation. For example in this study, a metal path is used to connect the ground faces of the two ports. This metal path induces extra currents and alters the results. Thus de-embedding procedure is needed to cancel this intervention.

In this work, the noise coupling through the substrate with a grounded backplane is studied, by means of a commercial simulator. Three different doping profiles are examined, which correspond to the ones commonly used in modern technologies. The impact of the doping profile to the noise coupling is considered in each case. Also the impact of using different metal layers is studied. The paper is organized as follows. In Section II the studied structures are presented. De-embedding procedure is analyzed in Section III. The simulation results of the comparison between the doping profiles and between different metal layers are presented in Section IV. Finally, section V concludes the work.

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II. SUBSTRATE STRUCTURES

The basic parameter that defines the noise transmission through the substrate is the conductivity. It is determined by adjusting the carrier concentration “p” and the hole mobility “ μ_p ”. Therefore, conductivity depends on the doping profile of the substrate.

The modern process technologies are categorized into three types. Firstly the memory and RF processes with a high resistivity substrate that consist the uniformly doped profiles. These profiles are used by all TSMC and UMC processes. Secondly the digital layer with a low resistivity substrate and a high resistivity epitaxial layer which consist the heavily doped profiles. These profiles are used for STMicro and IBM processes and optional for some TSMC and UMC processes. Lastly the bipolar processes with high resistivity substrate and epitaxial layer and low resistivity buried layers called the lightly doped profile. The lightly doped profile is used in IBM and STMicro technologies [2]. High resistivity substrates (HRS) are used for less loss in RF applications. In these applications noise isolation and minimization of eddy currents in the substrate are important to enhance the quality factor of all passive devices built on it that are critical for RF applications [3].

The three major doping profiles used in modern technologies correspond to a highly, a lightly (with a qualitatively opposite layer stack up) and a uniformly doped substrate [4]. Fig. 1 shows the typical layer stack up for the three main processes, along with their typical values in each case. In more detail, the lightly doped process includes a substrate with a relative high resistivity value of the order of 20 Ω cm. A highly conductive epitaxial layer exists above the bulk substrate having an average resistivity 10m Ω ·cm. In a highly doped substrate, the doping profile is qualitatively the opposite of the lightly doped one. In particular, it consists of a highly doped bulk having a resistivity value of about 1 m Ω cm. and a low conductive epitaxial layer above with an average resistivity value 20 Ω cm. The uniformly doped structure consists of a bulk and an epi layer of the same resistivity in the range of 10 Ω cm. The height of the corresponding layers in each process is roughly the same. Specifically, the height of the epi layer is about $h_e = 2\mu\text{m}$ and that of the bulk substrate ranges around $h_b = 300\mu\text{m}$. [5]. The difference in doping profiles between the two main processes affects the coupling mechanism and eventually the noise propagating through the substrate.

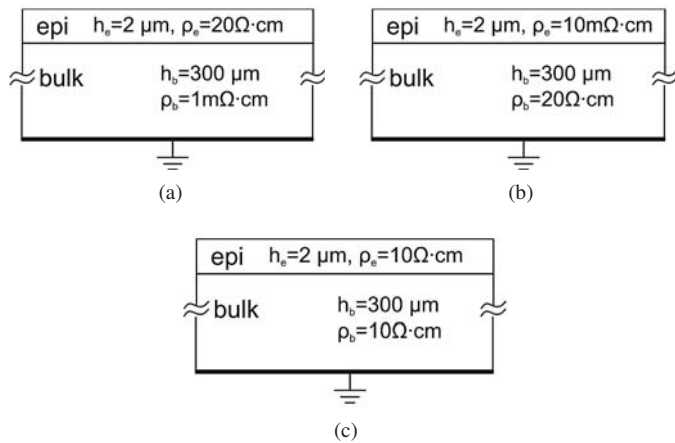
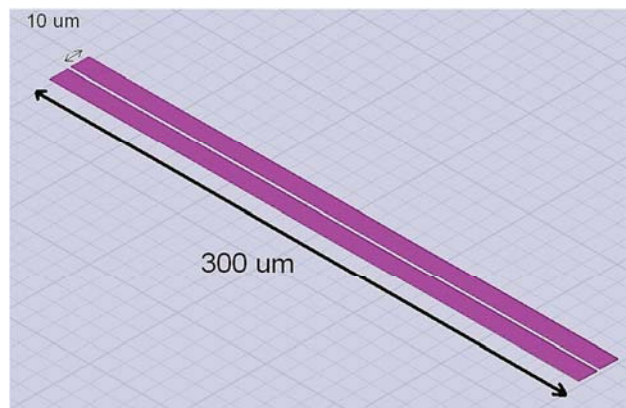


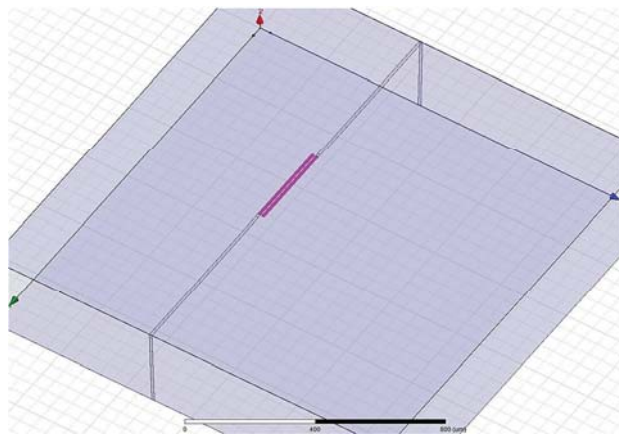
Figure 1. Doping profile of the layer stack-up of a (a) heavily doped process (b) lightly doped process and (c) uniformly doped process.

TABLE I. GEOMETRY OF THE INTERCONNECT STRUCTURE

Structure parameters	
Description	Value
Interconnect width	10 μm
Interconnect length	300 μm
Interconnect spacing	2, 20, 200 μm
Substrate width and length	1500 μm



(a)



(b)

Figure 2. (a) The parallel interconnects (b) The simulated structure with the ports and the connection to the ground plane.

The parameters of the interconnect structure, simulated by ANSYS HFSS, are shown in Table I. The two parallel interconnect lines, shown in Fig. 2(a), are connected via a metal path that leads to the ground and connects to the grounded plane of the substrate. This ring is required by the simulator in order to connect the excitation ports at the edges of the interconnect length, as shown in Fig. 2(b).

The substrate can be modeled by a two port π -resistance network [7]. Furthermore, other models exist, due to exact occasion of the modeled structure, such as an RLCG two parallel transmission interconnect line model or analytical models such as quasi-static (QS) and magnetic potential (MP) models [8-9]. In this study the extracted z and s parameters will be used for analysis, comparisons and conclusions.

III. DE-EMBEDDING OF SIMULATED DATA

In several simulators it is required to use a ground plane and/or a metal ring connection to the ground plane and between the excitation ports of the simulated structure. Thorough examination of the results can lead to the conclusion that the simulated structure, including the ring and the ground plane, alters the desired results of the interconnect interactions. A simplified de-embedding method is used in order to reduce this influence [10-12]. The formula that is used in this study is described in the following simplified expression:

$$Y_{DUT} = Y_{meas} - Y_{open} \tag{1}$$

whereas Y_{meas} is the matrix of the simulated y parameters of the structure in Fig 2(b) and Y_{open} is the matrix of the simulated structure without the two parallel interconnects. Table II shows the average error that occurs for each of the simulation results if no de-embedding procedure is applied. The maximum error in some cases was about 8% for Z_{11} and about 20% for Z_{12} .

TABLE II. AVERAGE ERROR WITHOUT THE DE-EMBEDDING PROCEDURE

Average errors for the various structures if no de-embedding procedure is applied		
Simulation	Z11 error	Z12 error
Heavily doped substrate with 2um distanced interconnects	2.84%	5.40%
Heavily doped substrate with 20um distanced interconnects	4.99%	9.44%
Heavily doped substrate with 200um distanced interconnects	5.12%	10.03%
Lightly doped substrate with 2um distanced interconnects	3.49%	6.29%
Lightly doped substrate with 20um distanced interconnects	2.80%	7.60%
Lightly doped substrate with 200um distanced interconnects	2.85%	10.99%

The difference between the de-embedded and the not de-embedded structure as well as the z parameter of the open structure are presented in figure 3. Therefore, in the following paragraphs all parameters were de-embedded before presented, in order to avoid unexpected results and faulty conclusions.

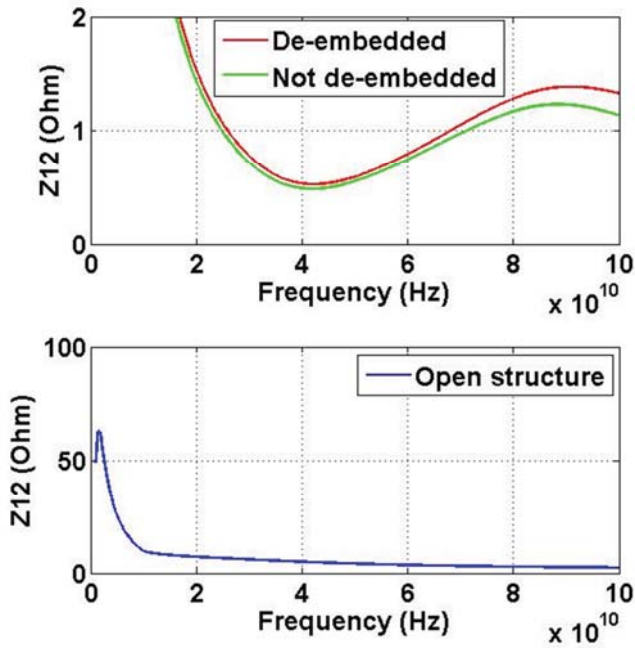


Figure 3. The de-embedded, the not de-embedded and the open structure Z_{12} parameters of lightly doped substrate structure with 20 μm distanced interconnections.

IV. SIMULATION RESULTS

A. Heavily doped structure

The s parameters of the heavily doped structure are presented in figure 4. The structure with the spacing of 20 μm between interconnections seems to have almost the same behavior as the 2 μm one. The S_{12} parameter expresses the signal that passes from the aggressor interconnect (port 2) to the victim (port 1). Thus, if S_{12} parameter is lower, then the impact of substrate noise coupling is lesser. As shown, a pair of 200 μm interconnections' spacing seem to have better isolation due to the S_{12} parameter.

B. Lightly doped structure

The s parameters of the lightly doped structure are presented in fig. 5. Two of the three structures have almost the same S parameters. Furthermore it is shown that the increase of the spacing between the interconnections lowers the S_{12} parameter, which indicates the increase of the isolation between them, similar to the case of the heavily doped procedure.

C. Uniformly doped structure

The s parameters of the uniform doped structure are presented in fig. 6. The two of the three structures, with interconnections' spacing 2 μm and 20 μm have almost the same S parameters. Moreover it becomes apparent that the increase of the distance between the interconnections lowers the S_{12} parameter, up to approximately 90 GHz. This shows the increase of the isolation between them, which is similar to the previous cases except for frequencies above 90 GHz.

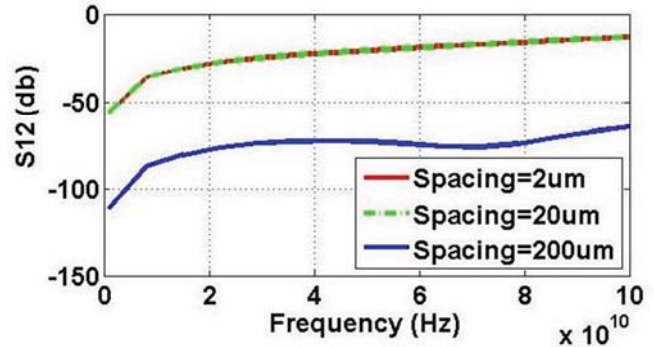


Figure 4. S parameters of heavily doped substrate structures of different interconnect distances.

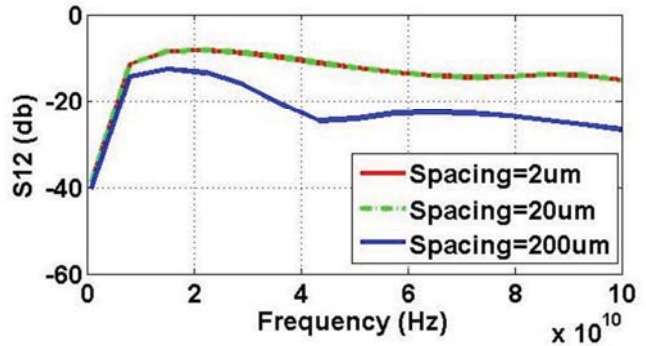


Figure 5. S parameters of various lightly doped substrate structures of different interconnect distances.

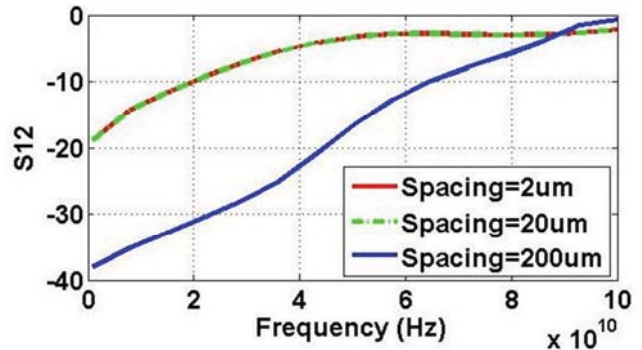


Figure 6. S parameters of various uniformly doped substrate structures of different interconnect distances.

D. Comparison of heavily, lightly and uniformly doped structures

Figures 7, 8 and 9 present the simulated S_{11} and S_{12} parameters that compare heavily, lightly and uniformly doped processes. The important impact of the various kind of doping processes can be observed in all three figures. As analyzed previously, the S_{12} parameter expresses the signal that passes from the one interconnect to the other. When S_{12} parameter is lower, then the impact of substrate noise coupling is lesser. As a result, for all three structures, heavily doped case offers better isolation.

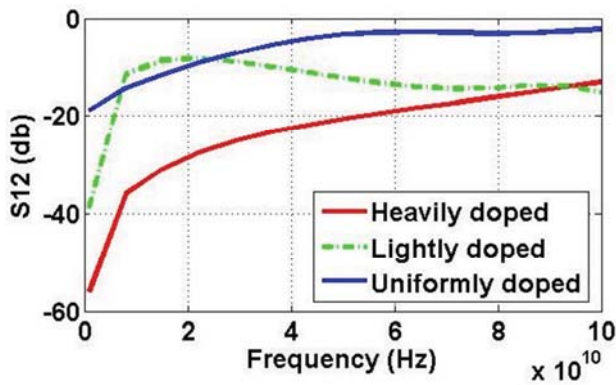


Figure 7. Comparison of S parameters of heavily, lightly and uniformly doped substrate structures for interconnect distance of 2um

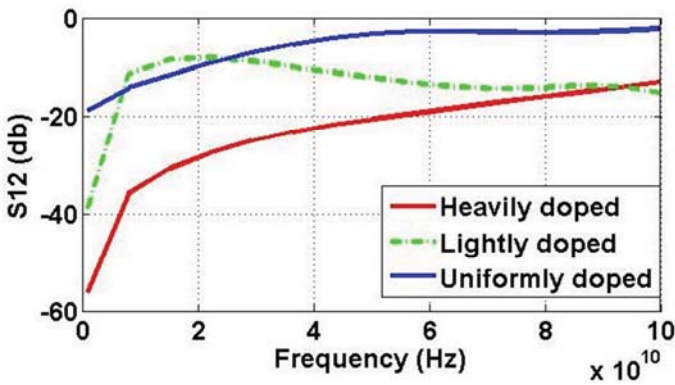


Figure 8. Comparison of S parameters of heavily and lightly doped substrate structures for interconnect distance of 20um

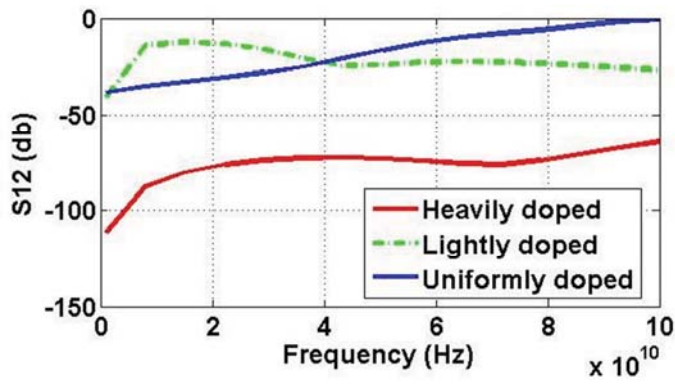


Figure 9. Comparison of S parameters of heavily and lightly doped substrate structures for interconnect distance of 200um

E. Comparison of Different Metal Layers

According to approximations regarding a 65nm CMOS technology, the parameters shown in Table III could describe the metal and oxide (ILD) layer thickness. These parameters were used to simulate two different cases, firstly assuming interconnect coupling on the first metal layer and secondly on the third metal layer. The behavior of the coupling mechanism in those structures commonly used in 65 nm CMOS technology was studied. The substrate noise coupling was examined between two interconnects of several distances. As shown in figure 10 when using Metal in layer 3, lower values of S12 parameters are achieved, proving better isolation and lower noise coupling. This happens in all three structures of

interconnect distances of 2um, 20um and 200um leading to the intuitive conclusion that the upper layers offer better isolation and higher tolerance to substrate noise coupling.

TABLE III. THICKNESS OF DIFFERENT LAYERS

Assumed layer thicknesses parameters	
Description	Value
M1 thickness	0.16 μm
Oxide1 thickness (M1 to substr.)	0.3 μm
M3 thickness	0.22 μm
Oxide3 thickness (M3 to substr.)	1 μm
Substrate thickness	300 μm

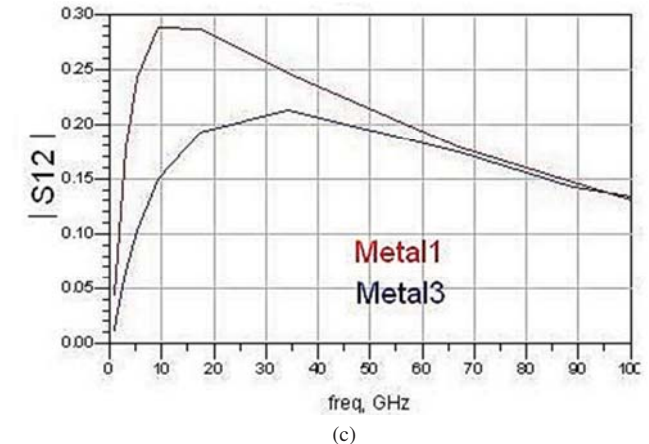
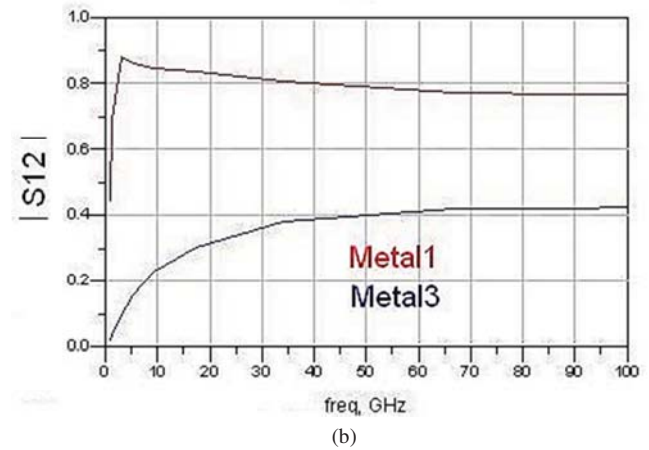
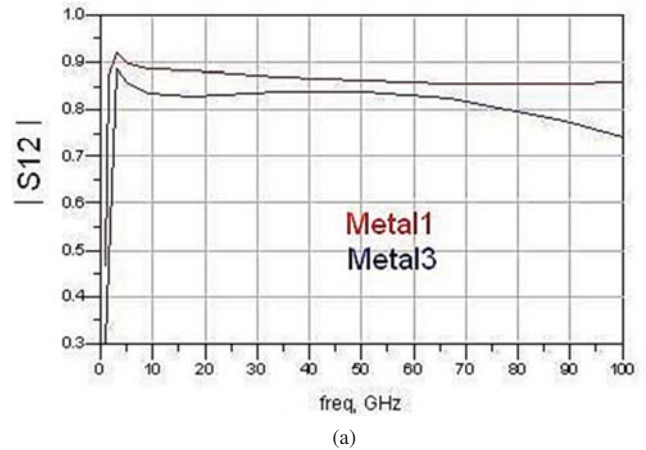


Figure 10. Comparison of S12 parameters of different metal layers for interconnect distance of (a) 2um (b) 20um (c) 200um.

V. CONCLUSIONS AND FURTHER WORK

The substrate noise coupling was studied in this work. Three different doping profiles were examined and their impact to the coupling level was investigated. Heavily doped substrate profile seems to offer better isolation for the elements of the structure at most cases. Also two different metal layers were utilized for the simulations. The need for de-embedding of the simulated data was revealed and a simplified de-embedding formula was implemented. Work is under way to study more cases and to construct a simple, fast and accurate model for describing the coupling in these cases.

REFERENCES

- [1] Jyh-Chyurn Guo and Yi-Min Lin, "A New Lossy Substrate De-embedding Method for Sub-100 nm RF CMOS Noise Extraction and Modeling" in IEEE Transactions on electron devices, Vol. 53, No2, February 2006, pp. 339-347.
- [2] Ahmed Helmy, Mohammed Ismail, "Substrate noise coupling in RFICs", Analog Circuits and Signal Processing series, Springer, 2008.
- [3] Wen Shu, Sam Shichijo and Rashaunda M. Henderson, "Loss Mechanism and High-low Doping Profile Effects of Silicon Substrate with Different Resistivities at High Frequency", Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International, pp. 1-4.
- [4] Hai Lan, Zhiping Yu and Robert W. Dutton, "A CAD-Oriented Modeling Approach of Frequency-Dependent Behavior of Substrate Noise Coupling for Mixed-Signal IC Design" in Proceedings of the 4th International Symposium on Quality Electronic Design (ISQED'03), 2003, pp. 195-200.
- [5] Gholan Reza Karimi and Ebrahim Akbari, "An efficient technique for accurate modeling and simulation of substrate coupling in deep micron mixed-signal ICs", International Conference on Electronic Devices, Systems and Applications (ICEDSA2010), 2010, pp. 88-92.
- [6] Harpreet Parashar and Ghanshyam Singh, "Effects of capacitive and inductive coupling on interconnects at RF Frequencies", Devices and Communications (ICDeCom), 2011 International Conference, pp. 1-5.
- [7] Ajit Sharma, Patrick Birrer, Sasi Kumar Arunachalam, Chenggang Xu, Teri S. Fiez, Kartikeya Mayaram, "Accurate prediction of substrate parasitics in heavily doped CMOS processes using a calibrated boundary element solver", IEEE Transactions on Very Large Scale Integration (VLSI) systems, vol. 13, No. 7, July 2005, pp. 843-851.
- [8] Madhumanti Datta, Susmita Sahoo, Rajib Kar, "Bandwidth Modelling for Distributed On-Chip RLCG Interconnect Considering Coupling Effects", International Conference on Devices and Communications (ICDECom), 2011, pp. 1-5.
- [9] Georgios Veronis, Yi-Chang Lu, and Robert W. Dutton, "Modeling of Wave Behavior of Substrate Noise Coupling for Mixed-Signal IC Design", Proceedings of the 5th International Symposium on Quality Electronic Design, 2004, pp 303-308.
- [10] Maria Drakaki, Alkis A. Hatzopoulos, Stylianos Siskos, "Improving the Accuracy of the De-embedding Methods for on-wafer RF Measurements", Elsevier Science Publishers, Microelectronics Journal, Volume 40, Issue 6, June, 2009, pp. 958-965.
- [11] Luuk F. Tiemeijer and Ramon J. Havens, "A Calibrated Lumped-Element De-Embedding Technique for On-Wafer RF Characterization of High-Quality Inductors and High-Speed Transistors", IEEE Transactions on electron devices, vol. 50, no. 3, pp. 822-829, Mar. 2003.
- [12] E. P. Vandamme, D. M. M.-P. Schreurs, and C. van Dinther, "Improved three-step de-embedding method to accurately account for the influence of pad parasitics in silicon on-wafer RF test-structures", IEEE Transactions on electron devices, vol. 48, no. 4, pp. 737-742, Apr. 2001.



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