Co-design of a Low-power RF Receiver and Piezoelectric Energy Harvesting Power Supply for a Wireless Sensor Node

Nuno Mancelos, Joana Correia, João P. Oliveira, and Luís B. Oliveira

***Abstract*—A low-voltage RF CMOS receiver front-end and an energy harvesting power circuit for a piezoelectric source are presented as a co-designed solution for a Wireless Sensor Node. A MOSFET-only wideband balun LNA with noise cancelling and a 0.6 V supply voltage is designed in conjunction with a passive mixer. The passive mixer operates in current mode, allowing a minimal introduction of voltage noise and a good linearity. The receiver front-end reaches a total voltage conversion gain of 31 dB, a 0.1-5.2 GHz bandwidth, an IIP3 value of -1.35 dBm, and a noise figure inferior to 9 dB. The total power consumption is 1.95 mW. The energy harvesting power circuit consists of an active full bridge cross-coupled rectifier followed by a low-dropout (LDO) regulator, and it is able to guarantee a power output of 6 mW with a regulated output voltage of 0.6 V, for typical vibration patterns.**

***Index Terms*—CMOS RF analog front-end; Low-voltage wideband balun LNA; Passive mixer; Piezoelectric Energy Harvesting; Active full bridge rectifier; LDO regulator**

I. Introduction

LOW-POWER receiver architectures used in analog front-end transceiver circuits are a good option to consider when overall consumption is a key factor. This is the case for Wireless Sensor Networks (WSN), where individual sensor nodes, Wireless Sensor Actuator Nodes (WSAN), must be energetically autonomous and communicate wirelessly with each other, sharing information regarding physical measurements of their environment made by their sensors and eventually sharing commands destined to their actuators [1].

The Low-IF receiver architecture features down-conversion to an intermediate frequency that is high enough to avoid problems related with flicker noise (that are a concern in the direct conversion architecture) and low enough to relax the filter specifications associated with channel selection [2]. This architecture allows a good performance at low-power consumption, which is the main constraint of the target application.

Since the wireless sensor nodes must be energetically autonomous and battery replacement increases maintenance costs, Energy Harvesting (EH) techniques are a very promising solution to power these nodes. Among existing EH techniques, a piezoelectric power source was chosen [3], with the residual energy source to be scavenged contained in ambient vibrations. Piezoelectric transducers are essentially ceramic wafers that exhibit piezoelectricity. This property consists in the creation of electrical charge in piezoelectric materials when they suffer mechanical strains, and it is reversible, meaning that an applied electrical field results in internal mechanical strain. When subjected to vibration, these transducers create a varying output voltage that must be rectified and regulated, in order to meet the application's power requirements. The scavenged energy can then be stored with a supercapacitor. Figure 1 presents a block diagram for the overall approach, including the Low-IF receiver architecture.

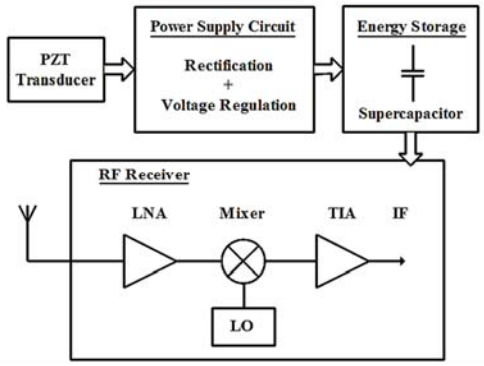

Fig. 1. Block diagram for this work's co-designed approach; Low-IF Receiver Architecture.

This work presents a CMOS low-voltage RF receiver front-end, which is designed to operate at a supply voltage of only 0.6 V and for simple binary modulations, such as OOK modulation [4]. The low-power consumption is possible due to a careful sizing of the transistors, the inclusion of low-voltage techniques in the LNA and the implementation of a passive mixer. The Dynamic Threshold voltage MOS (DTMOS) technique [5], was implemented in order to further reduce the operating supply voltage.

The EH power circuit, designed to power the RF receiver, includes an active full bridge cross-coupled rectifier that rectifies the output of the piezoelectric transducer. After the rectifier, a low-dropout (LDO) regulator is responsible for regulating the output of the rectifier to a *DC* voltage value of 0.6 V, with minimum ripple (<1%). The output of the power circuit feeds the receiver's power supply rail.

Section II presents a selection of relevant LNA and mixer circuits. The receiver proposed circuitry, including the LNA and mixer, is presented in section III. The piezoelectric EH system is introduced in Section IV. Section V presents the

This work was supported by national funds through FCT - Portuguese Foundation for Science and Technology under projects PEst-OE/EEI/UI0066/2011 and DISRUPTIVE (EXCL/EEI-ELC/0261/2012).

N. Mancelos, J. Correia, J. P. Oliveira and L.B. Oliveira are with CTS-UNINOVA, Department of Electrical Engineering (DEE), Faculty of Sciences and Technology (FCT), Universidade Nova de Lisboa, Monte da Caparica, Portugal (e-mails: n.mancelos@campus.fct.unl.pt, jm.correia@campus.fct.unl.pt, jpao@fct.unl.pt, l.oliveira@fct.unl.pt)

simulation results for the receiver, including gain, noise figure and linearity, and for the EH power circuit. Finally, some conclusions are presented in section VI.

II. Wideband Balun LNAs and Mixer Circuits

A. Wideband Balun LNAs

The wideband balun LNA presented in [6], and depicted in Fig. 2 has a common-gate (CG) and a common-source (CS) stage, a single-ended, unbalanced input and delivers a balanced output, thus guaranteeing the balun functionality. It is able to cancel the noise of the first stage, the CG-stage, as long as both stages have the same gain. This happens because the first stage's noise appears as a common-mode signal at the differential output. Dimensioning CG and CS devices with different sizes and bias allows this circuit to simultaneously benefit from noise and distortion cancelling and the output balancing abilities, as is demonstrated in [6]. The circuit can achieve very good linearity as long as the CS-stage's linearity is assured.

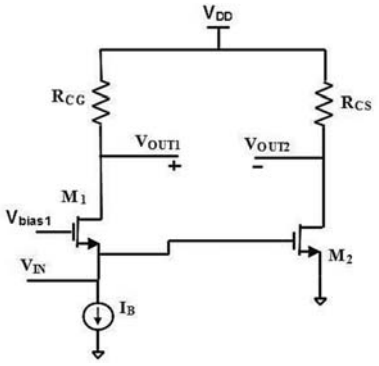

Fig. 2. Wideband Balun LNA [6].

A MOSFET-only version of the previously referred LNA circuit is presented in [7], Fig. 3. This version replaces the CG and CS resistors (used in [6]) by the PMOS transistors M_3 and M_4, respectively, operating in the triode region but close to saturation, allowing an increase to the incremental load resistance and, consequently, to the LNA's gain, for the same *DC* voltage drop. The replacement of the resistors by the PMOS devices also results in a reduction of circuit area and cost. Regarding the original LNA, this circuit has the disadvantage of an increased distortion and a reduction of bandwidth.

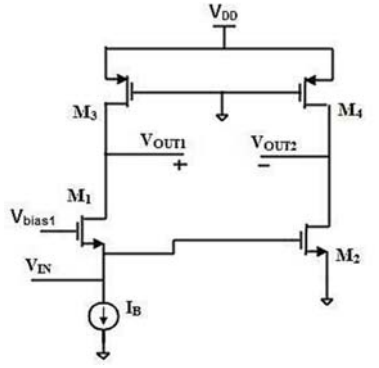

Fig. 3. MOSFET-only Wideband Balun LNA [7].

B. Mixer circuits

The simplest mixer configuration is a CMOS transistor-implemented switch, whose gate is driven by the Local Oscillator (LO) signal, with the RF signal being applied at its drain and the Intermediate Frequency (IF) signal being taken at its source. This passive mixer has no *DC* consumption and provides high linearity and bandwidth, [8].

Active mixers provide gain and strengthen the IF signal as they deliver it to subsequent receiver stages. They are most commonly based on the differential pair and can be single-balanced or double-balanced, depending on whether the RF signal coming from the LNA is balanced or unbalanced.

The single-balanced active mixer has a differential pair with the inputs driven by the LO signals and a current source controlled by the RF unbalanced signal. The two sides of the differential pair convert the RF input voltage to a current that is drawn alternately. For this mixer, the output spectrum includes the LO frequency. It is a simple active mixer that has moderate gain and noise figure, high input impedance, low 1 dB compression point, low IIP3 and low port-to-port isolation [8].

The double-balanced active mixer, called Gilbert cell, is more complex, having LO and RF differential inputs. It features improvements when compared to the single-balanced active mixer, namely higher gain, lower noise figure, high port-to-port isolation and good linearity. It is also able to remove the LO frequency from the output spectrum. These improvements come at the cost of higher consumption and increased circuit area and cost [1, 8].

III. Receiver Proposed Circuit

Figure 4 presents the complete circuit, including the LNA, mixer, *DC* decoupling capacitors between those two and the transimpedance amplifier (TIA), which is responsible for buffering the final output, low-pass filtering, and converting the current signal to a voltage signal. Between the mixer and the TIA a *DC* voltage source is added as a common-mode voltage of the two TIA inputs. The design of the TIA block is not detailed in this paper and the OTA is considered to reach a gain from 500 to 1000.

The main contribution of the presented circuit is not the introduction of new LNA and mixer architectures but rather the implementation of the current mode signal processing enabled by their combination. The RF signal coming from the antenna is converted to current and amplified by the LNA, being delivered to the mixer as a balanced signal. The mixer's output, a balanced current signal IF, is then converted to a balanced voltage signal by the TIA.

A. LNA

The proposed LNA circuit is presented in Fig. 4, along with the rest of the receiver analog front-end designed in the present work. This LNA is a new version of the MOSFET-only LNA presented in section II, designed to work at a supply voltage of 0.6 V. With a careful dimensioning, the use of the low-voltage DTMOS technique [5], and the introduction of independent stage biasing, the LNA is able to work without losing too much of its gain, as will be shown in section V.

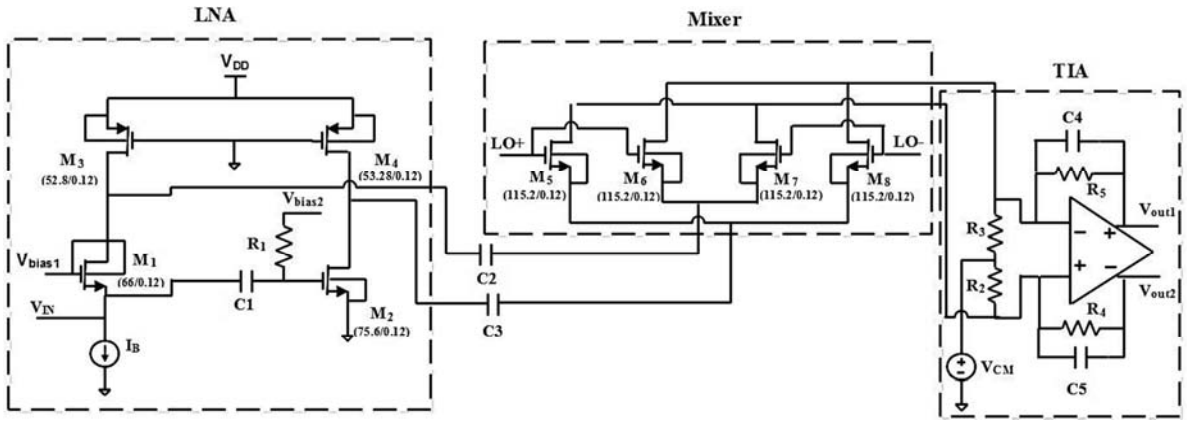

Fig. 4. Complete Receiver Circuit with all transistor sizes (W/L) in µm.

Since the dimensions of the PMOS devices can be adjusted to increase the LNA's output resistance, the current output of the LNA can be optimised. This is an important factor because the chosen mixer operates in current mode. Consequently, the LNA's voltage gain is not the main concern, but rather its transcondutance gain, which is essentially given by the M_1 (CG) and M_2 (CS) g_m values.

The V_{DD} reduction is possible due to an additional biasing voltage applied to the CS stage (V_{bias2}), to guarantee enough gate-source voltage across transistor M_2. Since V_{bias1} is limited to the supply voltage value, it wouldn't be sufficient to assure both M_1 and M_2 V_{GS} needed values. For this reason, V_{bias2} was added, along with the decoupling capacitor C_1.

Additionally, the DTMOS low-voltage technique is used in transistor M_1 to allow the low supply voltage operation. The technique consists in connecting the bulk of the transistor to its gate terminal, [5], introducing a dynamic regulation of the transistor's threshold voltage. The use of this technique allows enough drain-source voltage for the current-source transistor. It does so by reducing the threshold voltage of transistor M_1. The DTMOS technique is also responsible for a small increase in the effective *gm* of device M_1, slightly contributing to the CG voltage gain. This consideration is included in the LNA's differential voltage gain expression, (1), presented in this section.

LNA differential voltage gain

The expression for the LNA differential voltage gain is achieved by the subtraction of the CG and CS voltage gains, which were deduced using a small signal incremental model of the LNA. The gain is given by (1)

$$AV|_{Diff} = \frac{gm1+gmb1+gds1+gm2\left(\frac{g_{ds1}+g_{ds3}}{g_{ds2}+g_{ds4}}\right)}{g_{ds1}+g_{ds3}} \quad (1)$$

which can be approximated by (2).

$$AV|_{Diff} \approx \frac{gm1+gmb1+gm2}{g_{ds1}+g_{ds3}} \quad (2)$$

The presented approximation is valid considering that g_{ds1} and g_{ds2} have similar values, the same happening for g_{ds3} and g_{ds4}.

LNA input-impedance

The LNA input-impedance is given by (3).

$$Z_{in} = \frac{gds1+gds3}{(gm1+gmb1+gds1)g_{ds3}} \quad (3)$$

LNA noise figure

Assuming that $g_{m1} = g_{m2} = g_m$, the noise figure is given by (4) [6, 7].

$$F_{LNA} = 1 + \frac{k_f}{8kTR_S c_{ox} f^{\alpha f}}\left(\frac{1}{W_1 L_1} + \frac{1}{W_2 L_2}\right) + \frac{\gamma}{2R_S g_m} + \frac{1}{R_S r_{ds} g_m^2} \quad (4)$$

with k as the Boltzmann's constant, c'_{ox} the oxide gate capacitance per unit area, W_i and L_i the transistor dimensions, T the absolute temperature, γ the excess noise factor, k_f and α_f intrinsic process parameters.

B. Mixer

The choice of the mixer architecture for the receiver was governed once again by the energy consumption constraint of the target application and by the requirements of 0.6 V voltage supply. Since these factors are critical for the overall functioning of the WSAN receiver, a passive mixer architecture was chosen. The circuit is presented in Fig. 4 and consists of two pairs of NMOS transistors used as voltage-controlled switches, working in the triode region to maintain a low drain-source voltage when turned ON. The RF signal at the mixer's input is mixed in current. For a passive mixer as this one, the LO signals must be strong and buffered. The LO signals that drive the devices' gates are considered as ranging from 0 V to V_{DD} supply voltage, 0.6 V.

The mixer works in current mode, allowing a minimal introduction of noise and a good linearity. The reduced noise introduction, especially flicker noise, is possible due to the inclusion of the *DC* decoupling capacitors between the LNA and mixer, which guarantee there is no *DC* current flowing through the mixer. Moreover, due to the TIA, the variation of the drain-source voltage of the mixer's NMOS is reduced, thus contributing to improve the linearity of the circuit.

C. Theoretical expressions of the complete receiver circuit

Assuming that $g_{m1} = g_{m2} = g_m$ and $R_4 = R_5$, the noise figure is given by (5) [6, 7].

$$F_{Total} = 1 + \frac{k_f}{8kTR_S c_{ox} f^{\alpha f}}\left(\frac{1}{W_1 L_1} + \frac{1}{W_2 L_2}\right) + \frac{\gamma}{2R_S g_m} + \frac{1}{R_S R_4 g_m^2} \quad (5)$$

The overall conversion gain is given by (6).

$$CG_{Total} = Gm_{LNA+mixer} \times Z_{TIA\ Filter\ @\ 10MHz} \quad (6)$$

D. Receiver Circuit Sizing

The design process began by defining the V_{DD} voltage and power consumption values. V_{bias1} was set to 0.6 V and V_{bias2} at 0.45 V. A current mirror, biasing the first stage of the LNA with a current value of approximately 1.64 mA, was included as the current source. The common-mode voltage at the TIA input is set at 100 mV.

The circuit was dimensioned to work with an RF frequency of 1 GHz and an IF of 10 MHz. The LO frequency was considered as 990 MHz. For simulation purposes, the oscillator signals, LO+ and LO– in Fig. 4, were considered square waves in quadrature, with 50 ps of rise and fall times and without overlapping, with peak-to-peak buffered voltages of 0.6 V.

The NMOS and PMOS transistors chosen are RF transistors, with a triple-well structure chosen for the NMOS. Their dimensions are presented in Table I. The chosen length (L) for all the transistors was the technology's minimum L value, in this case 120 nm, in order to maximize circuit speed. To define the width for M_1, (3) was considered, so that this device's dimensions would guarantee 50 Ω input matching. Widths of M_3 and M_4 were determined by the LNA's output impedance, which means that these values were chosen with the objective of setting the PMOS drain-source resistances at a desired value, initially 200 Ω. The optimised value for the width of M_2 was chosen as the one which allowed the CS gain to match the CG gain, a required condition for the noise cancelling capability, as explained in section II. This matching of the CG and CS gains was possible after the optimization process applied to size M_2. The chosen width values for the mixer devices were set with the objective of achieving small drain-source resistance values.

The resistor and capacitor values chosen are presented in Table II. Resistor R_1 limits the *DC* current generated by V_{bias2} and resistors R_2 and R_3 help setting the common-mode voltage at the TIA input. Capacitor C_1 is responsible for the *DC* decoupling between the two LNA stages and capacitors C_2 and C_3 allow the *DC* decoupling between the LNA and mixer, while achieving low impedance values at the RF frequency of interest. Resistor values of R_4, R_5 and capacitor values of C_4 and C_5 are chosen so that a low pass filter is implemented at the TIA. The cutoff frequency of the filter was dimensioned to be slightly higher than the IF frequency, in order to attenuate frequencies above IF. The TIA's transresistance gain value, responsible for the current to voltage conversion, is 200 KΩ for the IF frequency (10 MHz). This value corresponds to the impedance of the parallel of resistor R_5 and capacitor C_4 (or R_4 and C_5) for the given IF frequency.

TABLE I.
TRANSISTOR DIMENSIONS FOR THE LNA AND MIXER

		I_D (mA)	W (μm)	L (μm)	r_{ds} (Ω)	g_{ds} (mS)	g_m (mS)
LNA	M_1	1.64	66	0.12	453	2.2	20.15
	M_2	1.63	75.6	0.12	576	1.73	21.88
	M_3	1.64	52.8	0.12	254	3.93	8.6
	M_4	1.63	53.28	0.12	257	3.89	8.5
Mixer	$M_{5,6,7,8}$	-	115.2	0.12	-	-	-

TABLE II.
RESISTOR AND CAPACITOR DIMENSIONS

	R1,R2,R3 (kΩ)	R4,R5 (kΩ)	C1,C2,C3 (ρF)	C4,C5 (ρF)
Values	10	200	5	9

IV. ENERGY HARVESTING PROPOSED CIRCUIT

Figure 5 presents a block diagram of the EH system, including the rectifier block, the voltage regulator block and the C_{rect} and $C_{storage}$ supercapacitors. The EH power circuit is responsible for the conditioning of the piezoelectric transducer's power output. This output may be considered as an *AC* power signal with a frequency that is equal to the vibration frequency. This power signal is periodic but not trivial to emulate, consisting of irregular voltage bursts and peaks. As an approximation, sine waves were used to simulate the power source, with the typical amplitude voltage values given in the datasheet for the Midé Volture™ piezoelectric transducers family, [9]. These transducer output values were used as a specification for the ideal voltage source of the transducer's equivalent circuit presented in [3], in its Thevenin equivalent version.

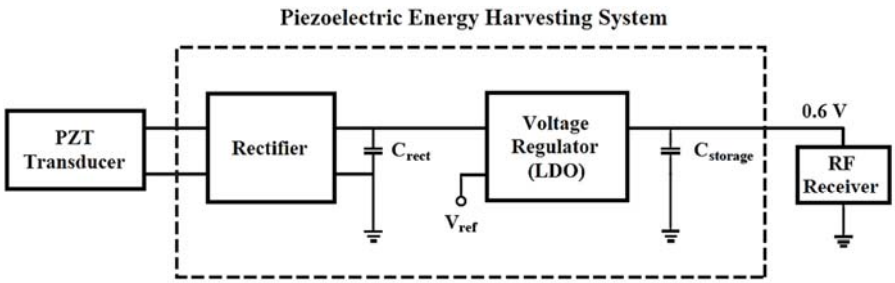

Fig. 5. Block Diagram of the Piezoelectric Energy Harvesting System.

The system was designed to work without batteries, making use of supercapacitors to store the scavenged energy. These supercapacitors are external components due to their high capacitance values, preferably higher than 100 μF. One of these, C_{rect}, is used at the output of the rectifier and is essential for the rectification. The $C_{storage}$ capacitor serves as the energy storage device, being placed after the voltage regulator. The 0.6 V regulated output of the system is taken directly at this capacitor's terminals.

Rectifier

The designed rectifier is an active full bridge cross-coupled rectifier, containing two NMOS and two PMOS transistors working as switches with their gates directly driven by the input terminals of the rectifier. Figure 6 shows the rectifier's schematic.

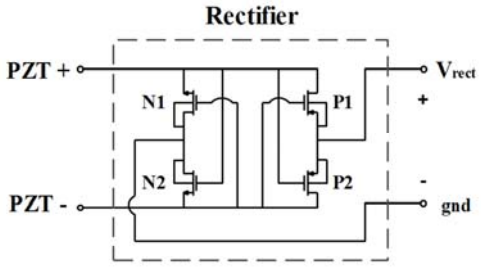

Fig. 6. Active Full Bridge Cross-coupled Rectifier Circuit Schematic.

The cross-coupled configuration allows the rectifier to behave as a full bridge rectifier. Having Fig. 6 as a reference, this means that transistors N1 and P2 are switched on while the rectifier's input is inverted, meaning that the PZT- terminal has a higher potential than the PZT+ terminal. When the opposite occurs, transistors N2 and P1 are on, because N2's gate is connected to the highest potential and P1's gate to the lowest. The rectifier's output terminals are connected to the C_{rect} capacitor and the rectifier charges this capacitor because this output's polarity is maintained during each period of the input signal. The anode terminal of the C_{rect} capacitor is called V_{rect}, since this is the node with the rectified voltage that needs to be regulated to a 0.6 V *DC* value. The cathode terminal represents the power circuit's ground.

A. LDO regulator

The LDO regulator acts as a DC-DC converter, regulating the V_{rect} output of the rectifier to a *DC* output at a constant 0.6 V. The output of the LDO regulator, V_{out}, is therefore connected to the $C_{storage}$ capacitor. The LDO regulator consists of a PMOS power switch and the comparator that drives the switch's gate. A schematic of the LDO regulator is shown in Fig. 7.

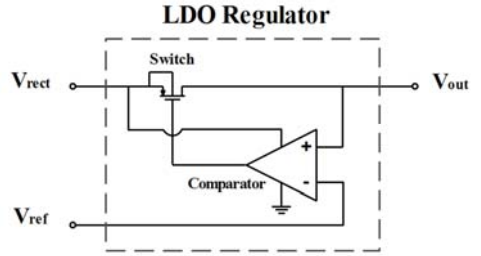

Fig. 7. Low-dropout Regulator Schematic.

The PMOS switch's source terminal is connected to V_{rect} and the drain terminal to V_{out}, which is the final output of the system presented in Fig. 5. The switch is on when V_{out} is below 0.6 V and it is off otherwise.

The design of the comparator was included in the design of the system, although it is not described in detail in this work; it is a latch comparator whose supply voltage terminal is directly connected to V_{rect}, allowing the comparator to have an internally generated voltage source and correctly drive the switch's gate. The non-inverting input of the comparator is connected to V_{out} and the inverting input is connected to an externally generated voltage reference of 0.6 V, V_{ref}. The comparator changes its output depending on the relation of the two inputs. If V_{out} is below 0.6 V, it means that the $C_{storage}$ capacitor needs to be charged in order to reach the desired output voltage, so the output of the comparator is set to 0 V, allowing the PMOS switch to connect the anode terminals of the two supercapacitors, which causes the C_{rect} capacitor to charge the $C_{storage}$ capacitor. When V_{out} is above 0.6 V, the switch must be turned off, so that the $C_{storage}$ capacitor does not continue to be charged. To guarantee the switch is turned off, the comparator changes its output to V_{rect}, which represents the highest potential at the terminals of the PMOS transistor, thus making the source to gate voltage approximately 0 V, turning the switch off. Since the load is constantly discharging the $C_{storage}$ capacitor, the voltage across this capacitor drops below the V_{ref} value afterwards, making the process repeat itself.

The frequency at which the comparator works was also dimensioned and its clock generator was designed to generate a clock at approximately 150 kHz. This frequency sets the speed at which the comparator compares its inputs and changes its output, and it highly influences the ripple value at the system's regulated output.

B. Energy Harvesting Power Circuit Sizing

The EH system may be seen as being constituted by two main parts: the power circuit and the control circuit. The control circuit corresponds to the comparator and clock generator circuits, whose implementation details and specifications are not addressed in this work. The power circuit consists of the blocks through which considerable currents flow, in the order of magnitude of tens of milliamps; these blocks are the rectifier and the switch. In order to withstand currents in that order of magnitude, these MOSFET transistors had to be dimensioned with large widths, and the multiplier factor was also regulated so that the high current could be split by several transistors in parallel, which also reduces the *rds* impedance. Table III presents the transistor dimensions for the rectifier and the PMOS switch.

TABLE III.
ENERGY HARVESTING POWER CIRCUIT SIZING

		W (μm)	L (μm)	m	$fingers$
Rectifier	N1	100	0.34	5	1
	N2	100	0.34	5	1
	P1	100	0.34	7	1
	P2	100	0.34	7	1
Switch	PMOS	50	0.34	6	2

V. Simulation Results

The circuits presented in this work were designed for a 130 nm CMOS technology and were simulated under SpectreRF using BSIM3v3 models.

A. Selection of simulations concerning the Receiver

For the IIP3 simulation, shown in Fig. 8, the tones are 100 MHz apart from each other, a situation that would be ideal for an IF frequency value of 100 MHz. Even though this is not the chosen IF frequency, the achieved results are also illustrative for a 10 MHz IF case. The simulation was run using a tone separation frequency value different from the desired IF frequency for reasons concerning simulation and convergence times. The IIP3 simulation renders a value of -1.35 dBm.

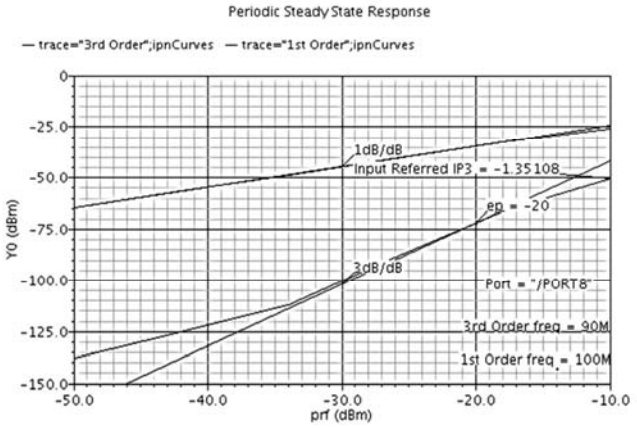

Fig. 8. IIP3 simulation.

In order to validate the low noise capabilities of the complete receiver circuit, a noise figure simulation, shown in Fig. 9, was run for the differential IF output. The simulation's results lead to the conclusion that the circuit presents a low noise figure, around 8.6 dB, for a relatively wide band of frequencies close to the desired IF frequency.

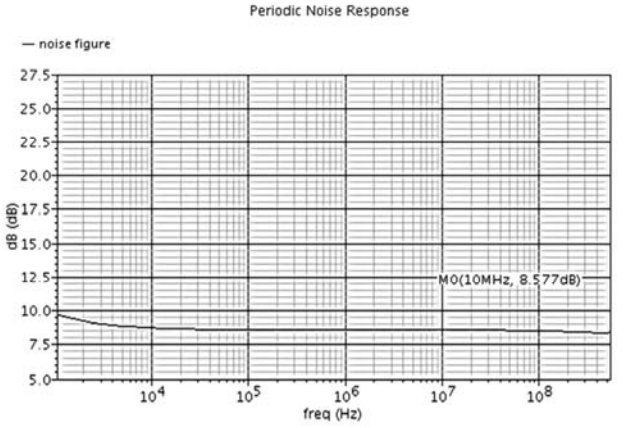

Fig. 9. Noise Figure simulation.

Results Table

Table IV presents the final results for this work's receiver circuit. These results include LNA bandwidth, LNA differential voltage gain, and some results for the complete circuit, namely conversion gain, noise figure, IIP3 and power consumption.

TABLE IV.
Final Receiver Simulation Results

Tech (nm)	LNA		LNA + Mixer				
	Band (GHz)	Gain (dB)	Voltage Conversion Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	VDD Supply (V)
130	0.1-5.2	17.6	31.5	<8.57	-1.35	1.95	0.6

FoM results and comparison with state-of-the-art circuits

The FoM expression considered is presented in (7). In order to calculate the FoM values, gain and NF were converted from the dB values presented in Tables IV and V.

$$FoM[\mathrm{mW}^{-1}] = \frac{AV|_{Diff}}{(NF-1)P_{DC}[\mathrm{mW}]} \quad (7)$$

For comparison purposes, the same FoM expression was used to calculate the state-of-the-art circuits' FoM values. A comparison with state-of-the-art LNAs is presented in Table V. The LNA was chosen for comparison because it is the most critical block in terms of gain and distortion in the receiver presented circuit.

TABLE V.
Comparison with State-of-the-Art LNAs.

Ref.	Tech (nm)	VDD (V)	Band (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	FoM (mW^{-1})
[6]	65	1.2	0.2-5.2	15.6	<3.5	>0	14	0.34
[10]	90	2.5	0.8–6	20	<3.5	>-3.5	12.5	0.6
[11]	90	1.2	0.1–1.9	20.6	<2.7	10.8	9.6	1.3
[12]	130	1.2	0.2–3.8	11.2	<2.8	-2.7	1.9	2.1
[7]	130	1.2	0.2–6.6	19.8	<1.8	1.6	4.8	3.9
This Work	**130**	**0.6**	**0.1–5.2**	**17.6**	**<5.2**	**2.3**	**1.95**	**1.7**

B. Energy Harvesting Power Circuit Simulations

To allow the EH power circuit to supply a fully functional receiver, an approximation was made for the total power consumption, and a *DC* current of 10 mA was considered as the load's total requested current, at a 0.6 V supply, which results in a total estimated power consumption of 6 mW.

For simulation purposes, a load (representing the receiver front-end) was added to the EH power circuit, consisting in a current mirror driving a *DC* current of 10 mA from the output of the system.

Figure 10 presents a transient simulation of the power circuit where the V_{rect} and V_{out} signals, specified in Fig. 6 and 7, can be seen. This simulation represents the charging process of the $C_{storage}$ capacitor, from which the 10 mA *DC* current is requested by the load. The voltage across the $C_{storage}$ capacitor, V_{out}, is initially 0 V and reaches the 0.6 V value after approximately 24 ms, for the chosen simulation conditions. The voltage ripple at the output is below 1%, as can be verified in the zoomed in section of Fig. 10. The piezoelectric transducer's electrical model, in its Thevenin equivalent version, has its ideal voltage source set to generate a sine wave with a 5 V amplitude value. The transducer presents a high internal voltage drop, which is why the rectifier's output, V_{rect}, presents a considerably lower value.

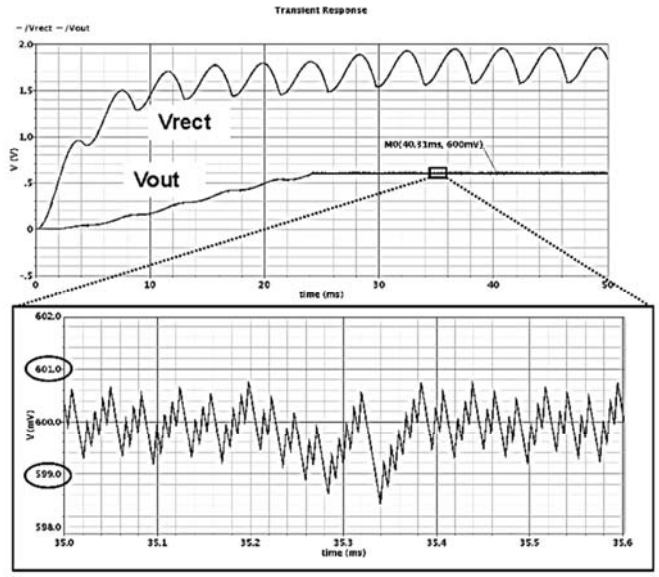

Fig. 10. Transient simulation for the Power Supply circuit; V_{rect} and V_{out} signals are specified in figures 6 and 7.

C. Results discussion

Regarding the Receiver

The receiver circuit's bandwidth satisfies the requirements for the target application. The LNA's voltage gain value is equivalent to the voltage gain value of the original MOSFET-only LNA that was considered, which is a positive result, having in mind the V_{DD} voltage supply reduction for the proposed circuit, in relation to the original one. The voltage conversion gain of the complete receiver circuit is a result of the contribution of the LNA's gain and the TIA's gain. The transimpedance gain of the TIA has a large contribution in this total conversion gain. The noise figure result is slightly higher than the LNA's noise figure, meaning that the mixer introduces some noise but not as much as an active mixer would. The IIP3 has a satisfactory value due to the reduced distortion introduced by the LNA and mixer.

The main advantages of the proposed receiver circuit are its low-power and low-voltage operation, its simplicity, good linearity and wideband operation, all of which are important factors for the target application. The introduction of noise is also reduced, thanks to the noise cancellation capability of the LNA and the fact that the receiver includes a passive mixer working in current mode. Moreover, it is an inductorless circuit, which helps in the reduction of the overall circuit area and, for that reason, circuit cost.

A disadvantage of the receiver circuit, which is a consequence of its simplicity, is its low Power Supply Rejection Ratio (PSRR). However, this disadvantage has its consequences taken to a minimum, because the power supply circuit is designed in order to deliver a strictly regulated voltage supply.

Regarding the Energy Harvesting Power Circuit

The EH power circuit is capable of guaranteeing a power output level that not only satisfies the LNA and mixer power demands but, eventually, the power requirements of the whole receiver. This is true for power outputs of the piezoelectric transducer obtained under relatively moderate periodic vibrations, as it occurs in certain industrial conditions where rotating machines are used. In case of non-constant vibrations, the sensor node enters into an intermittent operation mode where it wakes up only when the accumulated energy in the super-capacitor is enough for the operation of the overall system.

VI. Conclusions

The CMOS low-power and low-voltage RF receiver design includes the implementation of a MOSFET-only wideband balun LNA able to cancel noise and distortion, working at 0.6 V supply voltage, with a bandwidth of 0.1-5.2 GHz, a voltage gain of 17.6 dB, a noise figure inferior to 5.2 dB and an IIP3 value of 2.3 dBm. A double-balanced passive mixer is designed in conjunction with the LNA, working in current mode, and guaranteeing, together with the LNA and TIA, a total voltage conversion gain of 31.5 dB, an IIP3 value of -1.35 dBm, and a noise figure inferior to 9 dB. The total power consumption achieved is 1.95 mW.

A power consumption of 6 mW is guaranteed by the designed piezoelectric EH power circuit with an almost self-sufficient operation, considering that the piezoelectric transducer is subjected to moderate levels of vibration. This power supply is able to regulate the required voltage output with a ripple that is inferior to 1%, which is an important achievement, having in mind the receiver's low PSRR.

References

[1] K. Iniewski, "VLSI Circuits for Biomedical Applications," Artech House, 2008.

[2] J. Crols and M. Steyaert, "CMOS Wireless Transceiver Design", Kluwer, 1997.

[3] N. Mancelos, J. Correia, L.M. Pires, L.B. Oliveira, and J.P. Oliveira, "Piezoelectric energy harvester for a CMOS wireless sensor", *5th Doctoral Conference on Computing, Electrical and Industrial Systems (DoCEIS), Portugal, 2014.*

[4] C.C. Enz, N. Scolari, U. Yodprasit, "Ultra Low-Power Radio Design for Wireless Sensor Networks", *IEEE International Workshop on Radio-Frequency Technology,* Singapore, 2005.

[5] J. Correia, N. Mancelos, and J. Goes, "Stability improvements in a rail-to-rail input/output, constant gm operational amplifier, at 0.4V operation, using the low-voltage DTMOS technique", *5th Doctoral Conference on Computing, Electrical and Industrial Systems (DoCEIS), Portugal, 2014.*

[6] S. Blaakmeer, E. Klumperink, D. Leenaerts, and B. Nauta, "Wideband Balun-LNA with Simultaneous Outputs Balancing, Noise-Canceling and Distortion-Canceling", *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341-1350, June 2008.

[7] I. Bastos, L.B. Oliveira, J. Goes, M. Silva, "MOSFET-only wideband LNA with noise cancelling and gain optimization," *IEEE Mixed Design of Integrated Circuits and Systems (MIXDES)*, 2010, pp.306-311, 24-26 June 2010.

[8] L. Oliveira, J.R. Fernandes, I.M. Filanovsky, C.J.M. Verhoeven and M.M. Silva, "Analysis and Design of Quadrature Oscillators", Springer, 2008.

[9] Datasheet: Midé: Piezoelectric Energy Harvesters. Volture™.

[10] R. Bagheri, A. Mirzaei, S. Chehrazi, M.E. Heidari, M. Lee, M. Mikhemar, W. Tang, and A.A. Abidi, "An 800-MHz–6-GHz software-defined wireless receiver in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2860–2876, Dec. 2006.

[11] P.-I. Mak and R. Martins, "Design of an ESD-Protected Ultra-Wideband LNA in Nanoscale CMOS for Full-Band Mobile TV Tuners", *IEEE Trans. Circuits Systems I*, vol. 56, pp. 933-942, May 2009.

[12] A. Amer, E. Hegazi, and H. Ragai, "A low power wideband CMOS LNA for WiMax", *IEEE Trans. Circuits Systems. II*, vol. 54 nº 1, pp. 4-8, Jan. 2007.

Nuno Mancelos was born in Lisbon, Portugal, in 1989. He graduated in Electrical and Computer Engineering in 2012 at Faculdade de Ciências e Tecnologia (FCT), Universidade Nova de Lisboa (UNL), where he received the M.Sc. degree in Electrical and Computer Engineering, in 2014. In that same year he joined Silicon & Software Systems (S3) Group as a Mixed Signal Design Engineer. His research interests in microelectronics are in the areas of energy harvesting integrated power supplies, RF receivers and data converters.

Joana Correia was born in Lisbon, Portugal, in 1989. She graduated in Electrical and Computer Engineering in 2012 at Faculdade de Ciências e Tecnologia (FCT), Universidade Nova de Lisboa (UNL), where she received the M.Sc. degree in Electrical and Computer Engineering, in 2014. Her research interests are in the areas of the design of analog CMOS circuits for RF systems, in particular for low-power and low-voltage applications, and wireless sensor systems.

João P. Oliveira (S'95-M'97) was born in Paris, France, in 1969. He graduated in 1992 at Instituto Superior Técnico (IST) of the Technical University of Lisbon, where he also has received a M. Sc. degree in Electrical Engineering and Computer Science in 1996. He obtained the Ph. D. in 2010 from the New University of Lisbon (UNL). He has been with Department of Electrical Engineering of the Faculty of Sciences and Technology (FCT) of UNL as an Assistant Professor of microelectronics since 2003. Since 2004 he has been working as a Senior Researcher of the Centre for Technology and Systems (CTS) at UNINOVA. Since 2003 he has been a co-founder of MOBBIT Systems SA, a specialized system design Portuguese engineering company. From 1996 to 2003 he worked at the telecommunications industry in the area of 2G and 3G radio terminal equipment and switched packet data. Between 1992 and 1996, he was a Research Engineer at the Integrated Circuits and Systems Group (CGSI) at IST where he developed his work in the area of switched current-mode ADC and filters. His current research interests include, ultra-wideband radio, wireless sensor systems and mixed-signal integrated CMOS circuit design in digital technologies, namely, by using MOS parametric-based signal processing.

Luis B. Oliveira was born in Lisbon, Portugal, in 1979. He graduated in electrical and computer engineering and obtained the Ph.D. degree from Instituto Superior Técnico (IST), Technical University of Lisbon, in 2002 and 2007, respectively. Since 2001 he has been a member of the Analog and Mixed Signal Circuits Group at INESC-ID. Although this research work has been done mainly at INESC-ID, he has had intense collaboration with TU Delft, The Netherlands, and University of Alberta, Canada. In 2007, he joined the teaching staff of the Department of Electrical Engineering of Faculdade de Ciências e Tecnologia, Universidade Nova de Lisboa, and is currently a researcher at CTS-UNINOVA. His current research interests are in RF oscillators, PLLs, LNAs, Mixers, and other building blocks for RF integrated transceivers. Prof. Oliveira has several publications in international journals and leading conferences and he is the first author of "Analysis and Design of Quadrature Oscillators" (Springer, 2008).