Analysis and Simulation Modeling of Programmable Circuits Using Digital Potentiometers

Ivailo M. Pandiev

***Abstract*—In this paper an object of analysis and simulation modeling are the basic programmable circuits using CMOS digital potentiometers or Resistive Digital-to-Analog Converters (RDACs). Based on the analysis and principle of operation an improved SPICE – based behavioral model for RDAC potentiometers is created. The model accurately reflects resolution (wiper steps), nominal end-to-end resistance, wiper resistance, linear and nonlinear increment/decrement of the wiper, common-mode leakage current, operating bandwidth, analog crosstalk, temperature coefficients and noise effects. Model parameters are extracted for the dual RDAC potentiometer AD5235 from Analog Devices as an example. The workability of the proposed simulation model is verified by simulation modeling and experimental testing of sample electronic circuits.**

***Index Terms*—Mixed analogue digital integrated circuits, digital potentiometers, programmable circuits, frequency domain analysis, behavioral modeling, circuit simulation.**

I. Introduction

THE CMOS digital potentiometers (digital pots, digpots) or Resistive Digital-to-Analogue Converters (RDACs), as mixed (analogue and digital) integrated circuits, are important active building blocks for programmable analog circuits and devices. Most commonly the digital pots are used in a programmable voltage divider, which can be used to the offset compensation or the gain adjustment. The digital potentiometers are essential elements in the programmable amplifiers, attenuators, active filters, oscillators, circuits for offset compensation of the operational amplifiers (op amps), etc. Unlike the mechanical potentiometers in the CMOS digital pots the position of the middle point (wiper) *W*, towards to the both terminals *A* and *B*, is determined by using a digital code *D*. The main advantages of the digital pots in comparison with the mechanical pots are significantly smaller physical size, lack of mechanical wear or contamination of the wiper and low sensitivity to vibrations [1-4].

Most commonly the preliminary testing of the workability of electronic circuits and devices with digital pots are performed on breadboards. The software systems for automated analysis and design, such as Cadence OrCAD® are rarely used, because the majority of the mixed-signal elements do not have simulation models or macro-models. In [5] for some of the digital pots in its manufacturer's data a simplified simulation macro-model is given. Moreover, these macro-models reflected the dependence of the resistance *R* under the digital code *D* (specified in decimal form) and the parasitic capacitances at the both terminals – *A* and *B*. In 2010 the authors in [6] and [7] represent an improved simulation macro-model of a digital potentiometer. This macro-model uses as a basis the simplified equivalent circuit, as to it is added parallel resistor divider. This allows improving of the modeled frequency characteristic. Furthermore, in [7] a program DIGPOT to control digital potentiometers is presented.

This paper introduces new SPICE – based behavioral macro-model for the dual RDAC potentiometer AD5235 [8] as an example. The analysis of the available publications and the review of various mixed-signal ICs showed that this digital pot is a typical representative of the base structures, used for realization of RDAC potentiometers. The created macro-model for the digital pot AD5235 is implemented as a hierarchical block and the structure of its net-list confirm to the standard SPICE format.

The organization of the paper is as follows: the structures and the principles of operation of the RDAC potentiometers are described in section II; for the digital pots in section II the transfer function of the basic electronic circuits taking into account the parasitic capacitances of the terminals are given; in section III are illustrated the structure and the characteristic parameters of the proposed macro-model; in section IV examples of studying the created macro-model are presented and finally in section V the concluding remarks and directions for future work are discussed.

II. Structure of the RDAC Potentiometers and Theoretical Analysis

A. Structure and equivalent circuit of the RDAC potentiometers

One of the methods to obtain a digital potentiometer is like between the information inputs (with number 2^n) of an analogue multiplexer a 2^n-1 resistors with the same resistance *R* is connected. The first and last data input is indicated as terminals *A* and *B* of the potentiometer. The output of the analogue multiplexer is the wiper *W* of the potentiometer. These types of digital potentiometers are also known as RDAC potentiometers, where *n* is the number of bits and determined the resolution or "step size" of the digital

I. M. Pandiev is with the Department of Electronics, Faculty of Electronic Engineering and Technologies, Technical University of Sofia, 8 Kl. Ohridski Blvd, Sofia 1000, Bulgaria, (e-mail: ipandiev@tu-sofia.bg).

potentiometer with 2^n steps (positions) of the wiper. The simplified structure of *n*-bits RDAC potentiometer is given on Fig. 1. Other method to obtain variable resistors is to use a DAC with an additional current to voltage converter, and series resistor [1]. The main differences in comparison with the RDAC potentiometers are that in the variable resistors with DACs the wiper terminal is not defined and both terminals *A* and *B* are not electrically equivalent.

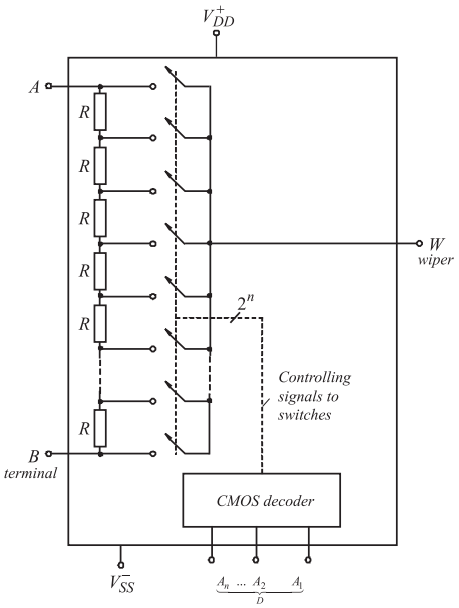

Fig. 1. Simplified circuit of *n*-bits RDAC potentiometer.

At applying a specific address (A_1, A_2, … A_n) to the decoder of the multiplexor one of the outputs of the decoder switch to logical '1', which causes the closing of one of the electronic switches. Thus, the wiper is positioned at one of the 2^n th points between terminals *A* and *B*.

Depending on the value of the binary code *D*, applied to the address inputs, the values of the resistances of the wiper *W* to terminal *B* and *W* to terminal *B* is given by

$$R_{WB}(D) = R_{AB}(D/2^n) \text{ and} \tag{1}$$

$$R_{WA}(D) = R_{AB}[(2^n - D)/2^n], \tag{2}$$

where $R_{WB}(D)$ is the resistance between W and B terminals, $R_{WA}(D)$ is the resistance between *W* and *A* terminals, and R_{AB} is the nominal resistance between *A* and *B* terminals.

Formulas (1) and (2) describe the behavior of an idealized model that is valid for d.c. and low frequencies applications. Logarithmic variation of the resistances R_{WA} and R_{WB} can be obtained by replacing *D* with 2^D.

Based on the structure of the RDAC pots (Fig. 1) an equivalent electrical circuit (Fig. 2) is obtained [1, 6]. It reflects the parasitic capacitances modeled by C_A, C_B and C_W, and the on-resistance of the electronic switches by R_W.

The parasitic capacitances C_A, C_B and C_W of all digital potentiometers can vary under change of the position of the wiper, as their values can vary from several *pF* to several tenths of *pF*. Moreover, the parasitic large capacitance value limits the working frequency bandwidth [7]. In general, the values of parasitic capacitances are function on the micro-electronic IC technology, the structure of the electrical circuit, the nominal resistance R_{AB} and the number of the steps of the wiper. In the datasheets for the majority of the digital potentiometers the values of the parasitic capacitances are usually defined only at the center position (i.e. code = half-scale) of the wiper. In some datasheets for digital potentiometers, such as AD8400 (from Analog Devices), are given formulas to calculate the concrete values of the parasitic capacitances at a given binary code:

$$C_A = \frac{D}{256}90pF + 30pF \text{ and}$$

$$C_B = \left(1 - \frac{D}{256}\right)90pF + 30pF .$$

At low frequencies (≤100*kHz*), for analysis and design of electronic circuits, the values of the capacitances at the half-scale of the wiper can be used. However, in practical point of view, it is better to use the largest values of the parasitic capacitances, which can most accurately ensure the specified bandwidth for all values of the binary code.

The noise performance of the digital pots can be represented, based of the definition of noise characteristics and analysis of IC data sheets. The resistors R_{AB} and R_W in OrCAD® PSpice A/D, generates equivalent thermal noise currents in parallel with the resistors (which is then noiseless). Alternatively, the equivalent thermal noise currents could be represented by mean-square voltage sources in series with the resistors with the level $\bar{e}_N^2 = \bar{i}_N^2 R_{AB}^2 = 4kTR_{AB}\Delta f$ (where k is Boltzmann's constant, T is the absolute temperature in °*K* and $\Delta f = f_{\max} - f_{\min}$ is noise bandwidth in Hertz).

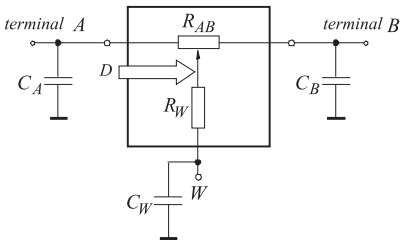

Fig. 2. Equivalent circuit of the digital pot model [1, 6].

The total rms noise signal that results at node *A* (or *B*) is the square root of the sum of the average mean-square value of the individual sources: $\bar{e}_{tot} = \sqrt{\bar{e}_{R_{AB}}^{-2} + \bar{e}_{R_W}^{-2}}$.

A sufficient degree of accuracy for the purpose of modeling the temperature dependence of the resistor R_{AB} has been provided by choosing $R_{AB}(T)$ as a linear temperature-dependent resistor ($TC2$ = 0), having the following characteristic equation [9]

$$R_{AB}(T) = R_{AB0}[1 + TC1(T - T_{nom})], \tag{3}$$

where R_{AB0} is the value of the resistor at $T_{nom} = 27°C$ (SPICE-Option TNOM), T is the temperature in $°C$ and $TC1$ is the linear temperature coefficient.

The value of the $TC1$ corresponds to the temperature coefficient of the resistance R_{AB} in IC data sheets.

B. Programmable circuits employing RDAC potentiometers and theoretical analysis

The electronic circuits of a programmable voltage divider with an output voltage follower (buffer) using op amp and a programmable non-inverting amplifier are the most commonly used circuits, into which occurs the effect of all elements of the equivalent circuit of the RDAC potentiometer shown on Fig. 2.

The basic circuit of programmable voltage divider with the output buffer is presented in Fig. 3. Including the equivalent circuit of the digital pot on Fig. 1 and linear model of the op amp [10] we get the a.c. equivalent circuit of the analyzed voltage divider. The $[Y]$-matrix of the circuit was composed using the well-known formulas [11], and after some transformations (using the condition $R_G << R_{WA}$, $A_d \to \infty$ and $r_{id} \to \infty$, where R_G is the internal resistance of the input voltage source u_i, A_d is the open-loop voltage gain and r_{id} is the differential input resistance of the op amp) we get the following expression for the transfer function

$$A_U(s) = \frac{1/R_{WA}R_W}{\left[\frac{1}{R_{WA}R_W} + \frac{1}{R_{WB|}R_W} + \frac{1}{r_{iA}}\left(\frac{1}{R_{WA}} + \frac{1}{R_{WB}} + \frac{1}{R_W}\right)\right]} \times$$

$$\times \frac{1}{\left[1 + s\frac{(C_W + C_{iA})\left(\frac{1}{R_{WA}} + \frac{1}{R_{WB}} + \frac{1}{R_W}\right)}{\frac{1}{R_{WA}R_W} + \frac{1}{R_{WB|}R_W} + \frac{1}{r_{iA}}\left(\frac{1}{R_{WA}} + \frac{1}{R_{WB}} + \frac{1}{R_W}\right)}\right]} = \frac{H_0}{1 + s/\omega_p}, \quad (4)$$

where r_{iA} and C_{iA} are the input resistance and input capacitance of the output buffer.

Comparison of the left and right sides of equation (3) results in the following formulas

$$H_0 = \frac{R_{WB}}{R_{WA} + R_{WB}} \frac{1}{1 + \frac{R_W}{r_{iA}} + \frac{R_{WAB}}{r_{iA}}} \text{ and} \quad (5a)$$

$$\omega_p = \frac{1}{(C_W + C_{iA})\frac{R_W + R_{WAB}}{1 + \frac{R_W}{r_{iA}} + \frac{R_{WAB}}{r_{iA}}}}, \quad (5b)$$

where $R_{WAB} = R_{WA} \| R_{WB}$.

In a.c. mode of operation formula (5a) define a low frequencies (at $\omega << \omega_p$) voltage gain of the voltage divider and formula (5b) define the value of the working bandwidth ω_{-3dB} at level $-3dB$. The bandwidth ω_{-3dB} determines the working frequency range and the stability of the digital pots.

In some of the previously proposed analyses of the equivalent circuit for the digital potentiometers [1]-[4], [7] are obtained formulas for the bandwidth and are discussed the effects of the various parasitic elements. However, in [1]-[4], the formula for the bandwidth not reflected the effect of the wiper resistance and the influence of the load. In [7] the variation of the bandwidth with regard to the parasitic capacitances and the position of the wiper are studied, but the formula in an analytical form is not given.

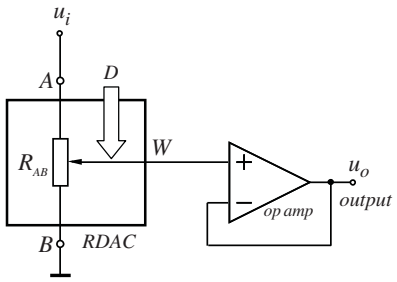

Fig. 3. Basic electronic circuit of programmable voltage divider using RDAC potentiometer and output buffer.

If $r_{iA} \to \infty$ and $\omega C_{iA} \to 0$ (for ideal output buffer) formulas (5a) and (5b) simplifies: $H_0 = R_{WB}/(R_{WA} + R_{WB})$ and $\omega_p = 1/(C_W + C_{iA})(R_W + R_{WAB})$.

From the analysis of formulas (5a) and (5b) for low frequencies ($f << f_p$) the voltage gain is equal to H_0 and the phase shift φ between the input and output signal is approximately equal to zero. For high frequencies ($f > f_p$) the gain is decreased to $|\dot{A}_U| \approx H_0 f_p / f$. Furthermore, the phase shift is $\varphi \to -90°$. That ensures the stable operation of the circuit in a wide frequency range, but in some applications for frequencies in which $f > f_p$ the additional phase shift between the output and the input signal can be cause on an unwanted effect. For example, if the circuit on Fig. 3 is used for volume control in multiple-channel audio power amplifiers [1-2] additional phase shift can affect on the stability of the output power stage.

For $A_d \neq \infty$ the working frequency bandwidth of the op amp needs to be 2 to 5 times larger than the cutoff frequency f_p. If in the circuit on Fig. 3, to extend the bandwidth, the buffer is removed the resistance r_{iA} and the capacitance C_{iA} will be the parameters of the load.

The well-known programmable non-inverting amplifier with digital pot in the negative feedback is shown on Fig. 4. In d.c. mode of operation the accuracy considerations for programmable amplifiers are somewhat more complicated than the ones for the amplifier circuits with a fixed voltage gain. This is because the transfer function is varying in a wide dynamic range according to the value of the binary code D. The accuracy for any combination of the binary code is determined from the total error. This is the deviation of the actual output

voltage $u_{out(actual)}$ from the ideal output voltage $u_{out(ideal)}$. Thus,

$$u_{out(actual)} = u_{out(ideal)} \pm u_{error}. \quad (6)$$

where $\pm u_{error}$ represents the sum of all the individual components (output offset voltage) of error normally associated with the amplifiers when working in d.c. mode of operation.

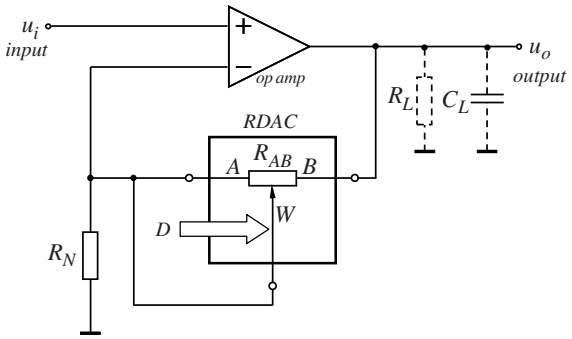

Fig. 4. A non-inverting amplifier circuit using RDAC potentiometer in negative feedback.

As with any transfer function, the error generated by the function itself may be referred to the output or to the input. The individual error components of programmable amplifiers are: input offset voltage U_{io}, input bias and leakage currents, as well as their temperature drifts. For most of the programmable amplifiers employing digital pots, the $u_{out(actual)}$ as a function of the major components of error can be found by

$$u_{out(actual)} = u_{out(ideal)} \pm \left[\left(1 + \frac{R_F}{R_N} \right) U_{io} + R_F I_B^- + R_F I_{LKGA} \right], \quad (7)$$

where the resistance R_F corresponds to the resistance R_{WB}, $I_B^- = I_{iB} - I_{io}/2$ is the input bias current of the inverting input of the op amp and $I_{LKGA} = I_{LKGB} = I_{LKG}/2$ is the leakage current at *A* and *B* terminals.

The leakage current is defined as current flowing from the node *W* on the condition, that to the node *W* a voltage $V_{DD}/2$ at the applied and the *A* and *B* terminals are no-connected.

When changing the ambient temperature the electrical parameters of the digital potentiometer and the parameters of the op amps are changed, as a result of this the u_{error} is increased:

$$|u_{err}| = \left[1 + \frac{R_F(1+\delta_R \Delta T)}{R_N(1 \pm \delta_R \Delta T)} \right] \Delta U_{io} + R_F(1+\delta_R \Delta T)\Delta I_B^- + $$
$$+ R_F(1+\delta_R \Delta T) I_{LKGA}, \quad (8)$$

where δ_R is the linear temperature coefficient of the resistors, $\Delta U_{io} = \partial U_{io}/\partial T$ is the temperature coefficient of the input offset voltage, $\Delta I_B^- = \partial I_B^-/\partial T$ is the temperature coefficient of the input bias current of the inverting input and $\Delta T = T - T_{nom}$.

In a.c. mode of operation the circuit the $[Y]$-matrix of the non-inverting amplifier was composed using the formulas given in [11], and after the transformations (using the condition $r_{id} \to \infty$) for the transfer function can be written

$$A_U(s) = \frac{\dfrac{A_{d0}}{R_F R_{p1}(C_{p1} + C_L^{'})C_N}\left(1 + \dfrac{R_F}{R_N}\right)}{s^2 + \left(\dfrac{1}{R_F(C_{P1} + C_L^{'})} + \dfrac{1}{R_{p1}(C_{P1} + C_L^{'})} + \right.} \times$$
$$\times \frac{(1 + sC_N R_F/(1 + R_F/R_N))}{\left. + \dfrac{1}{R_F C_N} + \dfrac{1}{R_N C_N} + \dfrac{1}{R_L(C_{p1} + C_L^{'})} \right) s + \dfrac{A_{d0}}{R_F R_{p1}(C_{p1} + C_L^{'})C_N}} =$$
$$= \frac{H_0(1 + s/\omega_z)}{s^2 + s(\omega_p/Q_p) + \omega_p^2}, \quad (9)$$

where $C_L^{'} = C_L + C_B + C_M$ (C_M is the parasitic board capacity with values usually up to $3pF$ [13]), $C_N = C_A + C_W + C_{id}^{+} + C_M$ ($C_{id}^{+} = C_{id} + C_{iCM}^{+}$ and $C_{iCM}^{+} \approx C_{iCM}^{-} = C_{iCM}/2$), R_{p1} and C_{p1} are the elements determined the dominant pole frequency ($f_{p1} = 1/2\pi(R_{p1}C_{p1})$) and A_{d0} is the d.c. open-loop voltage gain of the op amp.

Comparison of the left and right sides of equation (9) gives the formulas

$$H_0 = \frac{A_{d0}}{R_F R_{p1}(C_{p1} + C_L^{'})C_N}\left(1 + \frac{R_F}{R_N}\right) \quad (10)$$

– transmission coefficient,

$$\omega_z = 1/[(R_F \parallel R_N)C_N] \quad (11)$$

– angular zero frequency,

$$\omega_p = \sqrt{A_{d0}/[R_F R_{p1}(C_{p1} + C_L^{'})C_N]} \quad (12)$$

– pole angular frequency (complex pole or self-oscillating frequency) and

$$Q_p \approx \frac{\sqrt{A_{d0}}}{\sqrt{\dfrac{R_{p1}C_N}{R_F(C_{p1} + C_L^{'})}} + \sqrt{\dfrac{R_{p1}(C_{p1} + C_L^{'})}{R_F C_N}} +} \times$$
$$\times \frac{1}{+ \sqrt{\dfrac{R_F R_{p1}(C_{p1} + C_L^{'})}{R_N^2 C_N}} + \sqrt{\dfrac{R_F R_{p1} C_N}{R_L^2(C_{p1} + C_L^{'})}}} \quad (13)$$

– quality factor.

After substitution of $s = j\omega$ in formula (9) for the general complex transfer function is found

$$\dot{A}_U(j\omega) = \frac{H_0(1 + j\omega/\omega_z)}{\omega_p^2 - \omega^2 + j\omega\dfrac{\omega_p}{Q_p}}. \quad (14)$$

The module and the phase of the general complex function (14) for the non-inverting amplifier are

$$|\dot{A}_U(j\omega)| = A_U(\omega) = \frac{H_0\sqrt{1+\omega^2/\omega_z^2}}{\sqrt{\left(\omega_p^2-\omega^2\right)^2 + \left(\omega\dfrac{\omega_p}{Q_p}\right)^2}} \text{ and} \quad (15a)$$

$$\varphi_{A_U} = \arctan\left(\frac{\omega}{\omega_z}\right) - \arctan\frac{\omega_p\omega}{Q_p(\omega_p^2-\omega^2)}. \quad (15b)$$

The analysis of formulas (9), (15a) and (15b) shows that the transfer function is characterized by a double-pole with angular frequency equal to ω_p and one real zero with angular frequency – ω_z. However, for $\omega = 0$ the voltage gain has a value $A_{U0} = \dfrac{H_0}{\omega_p^2} = 1 + \dfrac{R_F}{R_N}$, while for much higher frequencies the gain decreases to zero. Therefore, the transfer characteristic of the programmable non-inverting amplifier circuit is a low-pass type.

For $Q_p \geq 0.707$ at a frequency equal to ω_p the denominator tends to zero and the voltage gain theoretically increases toward infinity. As a result, occurs peaking the frequency characteristic and the phase shift between the input and output signal increases rapidly to 180°. Moreover, the circuit of the non-inverting amplifier becomes unstable. In the cases where $Q_p < 0.707$ and $\omega_p < \omega_z$ the frequency response monotonically decreasing and the phase shift decreases to $-90°$. At $\omega_z < \omega_p$ occurs ringing in the output signal, which can cause unstable operation.

For chosen op amp and resistors in the negative feedback the values of poles and zeros are obtained. Based on these values at $|A_U(j\omega)|$ equal to $1/\sqrt{2}$, after some transformation of the complex function for the bandwidth ω_{-3dB} is obtained

$$\omega_{-3dB} = \frac{\omega_p^2}{\omega_z}\sqrt{1 + \left(1 - \frac{1}{2Q_p^2}\right)\frac{\omega_z^2}{\omega_p^2} + \sqrt{\left[1 + \left(1 - \frac{1}{2Q_p^2}\right)\frac{\omega_z^2}{\omega_p^2}\right]^2 + \frac{\omega_z^4}{\omega_p^4}}}. \quad (16)$$

At $Q_p = 1/\sqrt{2}$ formula (16) simplifies and yields

$$\omega_{-3dB} = \frac{\omega_p^2}{\omega_z}\sqrt{1 + \sqrt{1 + \frac{\omega_z^4}{\omega_p^4}}}. \quad (17)$$

For $\omega_z >> \omega_p$ and $Q_p = 1/\sqrt{2}$ $\omega_{-3dB} \approx \omega_p$.

On the theory and design of the amplifier circuits using op amps are dedicated relatively large number of books, publications and application reports. In the available literature [10]-[12], [14]-[18] the working frequency bandwidth is determined basically by the depth of the negative feedback without taking into account the poles and zero locations, determined mainly by the equivalent input capacitance C_N and the load capacitance C_L.

The magnitude and phase Bode plots for the loop gain at $\omega_z < \omega_p$ of a non-inverting amplifier employing digpot equivalent circuit (Fig. 2) is shown on Fig. 5. The Bode plots are constructed by summing the corresponding logarithmic characteristics of all their sections, realizing zeros and poles:

$$L(\omega) = 20\lg A_U(\omega) = \sum_{i=1}^{n} L_i(\omega) \text{ and} \quad (18a)$$

$$\varphi_{A_U}(\omega) = \sum_{i=1}^{n} \varphi_i(\omega), \quad (18b)$$

where $L_i(\omega)$ are the individual logarithmic magnitude characteristics ($L_1 = 20\lg H_0$, $L_2 = 20\lg(1 + s/\omega_z)$ and $L_3 = 20\lg[s^2 + s(\omega_p/Q_p) + \omega_p^2]^{-1}$) and $\varphi_i(\omega)$ are the individual phase characteristics ($\varphi_2 = \arctan\left(\dfrac{\omega}{\omega_z}\right)$ and $\varphi_3 = -\arctan\dfrac{\omega_p\omega}{Q_p(\omega_p^2-\omega^2)}$).

Formulas (10), (11) and (12), and Bode plots on Fig. 5 show the following:

a) For $A_{U0} \leq \sqrt{\omega_{B1}R_F C_N}$, there is always causes peaking in the magnitude plot and a rapid phase shift ($\geq 90°$) in the phase plot for the loop gain at a frequency approximately equal to ω_p. By increasing the d.c. voltage gain A_{U0} the zero frequency ω_z increases, whereby the amount of peaking in the frequency response decreases;

b) The phase margin ($|\varphi_m| = 180° - |\varphi_1|$, where $|\varphi_1|$ is the absolute value of the phase shift of the output signal at $|\dot{A}_U| = 1$) of the non-inverting amplifier is greater than 45°. However the stability of the circuit is worse. For a given frequency of the input signal, at which the asymptotes L_2 and L_3 intersect, the rate of the change of the voltage gain is about $40dB/dec$. The spikes in the magnitude plot leads to an increase of the amplitude of the output signal, which may adversely effect on the next stages and sections of the electronic devices and systems.

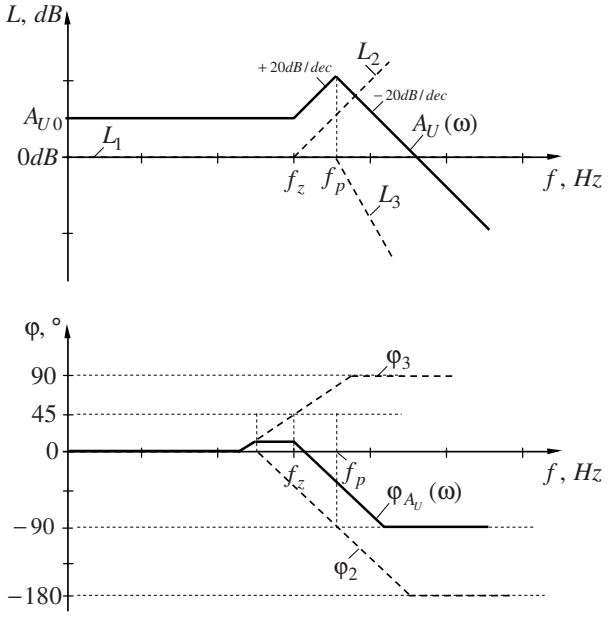

Fig. 5. Magnitude and phase Bode plots for the loop gain of a non-inverting amplifier employing digital pot equivalent circuit on Fig. 2.

III. Macro-model Description

"Perfection is achieved, not when there is nothing more to add, but when there is nothing left to take away."

Antoine de Saint-Exupery

The technical requirement for effective models is generally agreed when the simplest possible model is developed. Simple models have a number of advantages. They can be developed faster, are more flexible, require less data, run faster and it is easier to interpret the results since the structure of the model is better understood. As the complexity increases these advantages are lost [19].

One method to decrease simulation time and improve the convergence, without a significant loose of information, is by using behavioral modeling technique. Behavioral modeling is a way of providing macroscopic models of the corresponding microscopic (microelectronic) circuits. The use of behavioral modeling for analogue and mixed-signal devices has been well known for a few years. Behavioral models are realized by using structural macro-modeling, the C code modeling, VHDL-AMS and finally the analogue behavioral modeling (ABM) available in OrCAD® PSpice A/D. The proposed simple macro-model of RDAC pots basically use elements and primitives from the standard ABM library. The main advantages of the ABM technique are the portability to all SPICE simulators and also the user's access to the macro-model's internal equations and variables. The of RDAC pot macro-model is developed following the design methodology presented in [20] and applying simplification and build-up technique, known from modeling common operational amplifiers [21].

The circuit diagram of the proposed model is shown on Fig. 6a of dual RDAC potentiometer is presented as a hierarchical block (HB_RDAC). There are two sections. The model parameters of the blocks are given without concrete numerical values. During the modeling of a particular IC the numerical values are obtained. The functional block model of a digital pot is shown on Fig. 6b. Logarithmic variation of the wiper can be obtained by replacing @D1 (and @D2) in the formulas for the resistances $R_{WA1(2)}$ and $R_{WB1(2)}$ with PWRS(2,@D1) (and PWRS(2,@D2)).

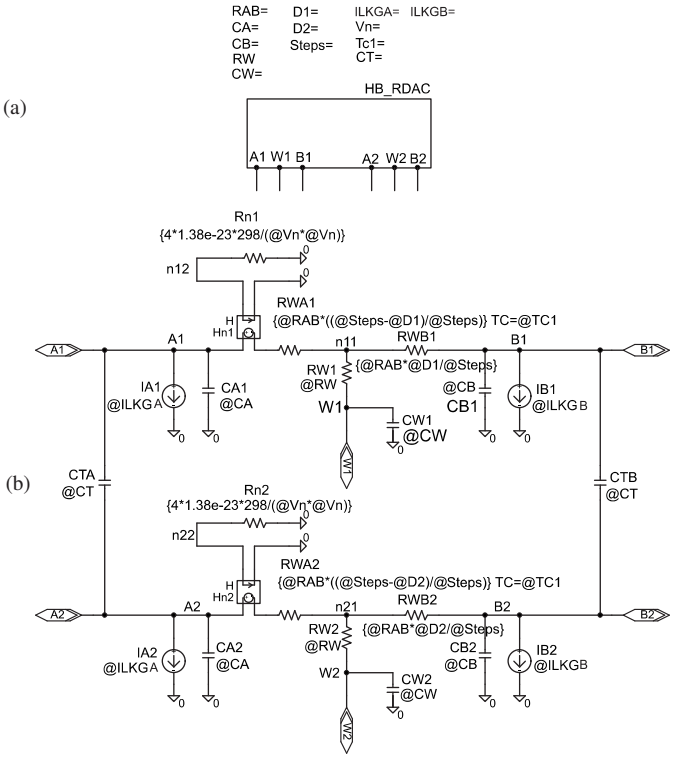

Fig. 6. The proposed behavioral macro-model of a dual RDAC potentiometer. (a) Circuit diagram. (b) Functional block.

In comparison with the equivalent circuit on Fig. 1 in the functional block on Fig. 6b to reflect the analog switches noise effects is added noise stages includes current-controlled voltage sources and parallel resistances with value $R_n = 4\times k\times 298°K/(V_n\times V_n)$. The *rms* voltage $\bar{e}_{N_o} = V_n$ is the white noise and can be found by $\bar{e}_{N_o} = \sqrt{\bar{e}^2_{N,DS} - \bar{e}^2_{N,\mathrm{Re}s}}$, where the *rms* voltage $\bar{e}_{N,DS}$ is the datasheet value of the white noise and the *rms* voltage $\bar{e}_{N,\mathrm{Re}s}$ is the white noise generated by large-value resistors commonly used in the macro-models. Also to *A* and *B* terminals are added ideal current sources ($I_{A1(2)}$ and $I_{B1(2)}$) modeling the leakage current at absence of input signal. The terminal parasitic capacitances are modeled with C_A and C_B, and the capacitors C_{TA} and C_{TB} produces the frequency dependence of the analog crosstalk ratio. The analog crosstalk is defined as a ratio between W_2 and A_1, if to the node A_1 an a.c. voltage V_{A1} is applied, terminal B_1 is connected to ground and terminals A_2 and B_2 are no-connected. In this mode of operation there is some penetration of the input a.c. signal through the capacitor C_T. The analog crosstalk ratio (*ACR*) of the macro-model can be calculated with

$$ACR \approx 20\lg(CT/CA). \tag{11}$$

The model parameters for RDAC potentiometer AD5235 from Analog Devices, used as an example in this paper, are: $R_{AB1(2)} = 25k\Omega$ and $250k\Omega$; $R_{W1(2)} = 50\Omega$; $Steps = 1024$; $C_{A1(2)} = C_{B1(2)} = 11pF$ (at half-scale); $C_{W1(2)} = 80pF$ (at half-scale); $C_T = 0.980fF$; $TC1 = 15ppm/°C$ and $I_{LKGA} = I_{LKGB} = 5nA$. The binary codes D_1 and D_2 are set as a global parameter for simulation testing and can take values from 1 to 1023.

IV. Macro-model Performance and Discussion

The workability of the proposed macro-model on Fig. 6 is presented through simulation results using the OrCAD® PSpice simulator built in Cadence OrCAD® and also through experimental results from the electronic circuits configured on prototype boards. The power supply voltages are chosen to be $\pm 2.5V$.

The verification check of the proposed macro-model, shown Fig. 6, is performed by comparing the simulation results with the datasheet parameters of digital pot AD5235. The test circuits for simulation modeling are created following the test conditions given in the semiconductor data books of the corresponding IC. In Table 1 the simulation results and the data sheet parameters for IC AD5235 are presented. Notice that the average error between the proposed macro-model and datasheet parameters is not higher than 5%, which guarantee the correct degree of accuracy.

To validate the proposed model, simulation and experimental test of programmable voltage divider (Fig. 2) and a programmable non-inverting amplifier (Fig. 3) was performed. In particular the experiments are performed on the EVAL-AD5235EBZ – Development board [22], which is built around the CMOS AD5235 device with $25k\Omega$ and $250k\Omega$ nominal resistance. For the non-inverting amplifier the values of the calculated passive components are: $R_N = 10k\Omega \pm 1\%$ (with $25ppm/°C$), $R_F = R_{WB} = 62.5k\Omega$ at $D = 256$ ($A_{U0} = 7.25$); $R_F = R_{WB} = 125k\Omega$ at $D = 512$ ($A_{U0} = 13.5$); and $R_F = R_{WB} = 187.5k\Omega$ at $D = 768$ ($A_{U0} = 19.7$).

TABLE I
Comparison between simulation results and data sheet parameters

Parameter	AD5235 data sheet [8]	The proposed digital pot macro-model
Resolution	10	10
Wiper resistance	50	50
Common-mode leakage current	10n*A*	10n*A*
Capacitance at *A* and *B*	11p*F*	11p*F*
Capacitance at *W*	80p*F*	80p*F*
Bandwidth at –3*dB*	32k*Hz* at 250kΩ 310k*Hz* at 25kΩ	32.2k*Hz* at 250kΩ 316k*Hz* at 25kΩ
Analog crosstalk	–81*dB* at 25kΩ	–80*dB* at 25kΩ
Temperature coefficient	15 ppm/°*C*	15.1 ppm/°*C*
Resistor noise density	20n*V*/√*Hz* at 25kΩ 64n*V*/√*Hz* at 250kΩ	20.3 n*V*/√*Hz* at 25kΩ 64.3n*V*/√*Hz* at 250kΩ

For the investigated circuits as an active element AD820AR (from Analog Dev.) is used. The simulation modeling of the circuits using AD820/AD SPICE macro-model, version A (08/1991) was performed. The basic modeled parameters of the AD820 SPICE macro-model at $V_S = \pm 2.5V$ and $R_L = 100k\Omega$ are: $U_{io} \approx 160\mu V$, $I_{io} = 2pA$, $I_{iB} = 6pA$, $r_{id} = 10^{13}\Omega$, $C_{id} = 5pF$, $r_{iCM} = 10^{13}\Omega$, $C_{iCM} = 10.8pF$, $A_{d0} = 120.1dB$, $f_{p1} \approx 1.8Hz$, $B_1 = 1.6MHz$, $\varphi_m \approx 63°$, $U_{om}^{+} = -U_{om}^{-} = 2.48V$, $\overline{S}_{U0} = 12nV/\sqrt{Hz}$ at $f = 0.01...10kHz$, $SR \approx 3.1V/\mu s$, $t_s = 1.8\mu s$ (at 0,01% peaking of the input signal) and $r_o = 40\Omega$ (the output impedance $Z_o = 44k\Omega$ within the range from d.c. to $1Hz$). The AD820 SPICE macro-model is not capable of simulating the noise, the temperature effects and some of the other second-order effects.

To obtain the a.c. transfer characteristics through simulation an AC sweep analysis is performed within OrCAD® PSpice. The AC sweep analysis causes an AC sweep to be performed on the circuits. AC sweep is a frequency response analysis. PSpice calculates the small-signal response of the circuit to a combination of inputs by transforming it around the bias point and treating it as a linear circuit. For the AC sweep analysis specified in Fig. 3 and Fig. 4, the frequency is swept from $1Hz$ to $10MHz$ by decades, with 100 points per decade. The input voltage source is with amplitude $100mV$ and initial phase shift equal to zero. The a.c. transfer characteristics of the circuits are obtained experimentally by using of function generator – SFG-2010, digital storage oscilloscope – TDS1012B and Instek GFC-8010H frequency counter.

For the programmable voltage divider at $D = 512$ the transfer characteristics are plotted on Fig. 7. The comparative analysis of the obtained frequency responses and transfer function, given (4), results in the following conclusions. For $f = 0$ the voltage gains A_{U0} are with constant value and corresponds to formula (5a). This remains applies to frequencies $f << f_p$, which means that the logarithmic characteristic is a straight line almost parallel to the x-axis. At a frequency $f = f_p$ the according to formula (5b) is $A_{U0} - 3dB$, i.e. it decreased by $3dB$ compared to its value at $f = 0$. The simulated values of the pole frequencies are $f_{p1} = 316kHz$ at $R_{AB} = 25k\Omega$ and $f_{p2} = 32kHz$ at $R_{AB} = 250k\Omega$. At frequencies $f >> f_p$ the transmission coefficient decreased approximately $-20dB/dec$. Therefore, in a logarithmic scale at $f >> f_p$ the frequency characteristic is approximated by a straight line that has a slope $-6dB/dec$ (or $-20dB/dec$). The difference between simulation results and experimental studies in the frequency range from $10Hz$ to $10MHz$ is less than 5%, which confirms the correctness of the theoretical analysis and the accuracy of the proposed behavioral model.

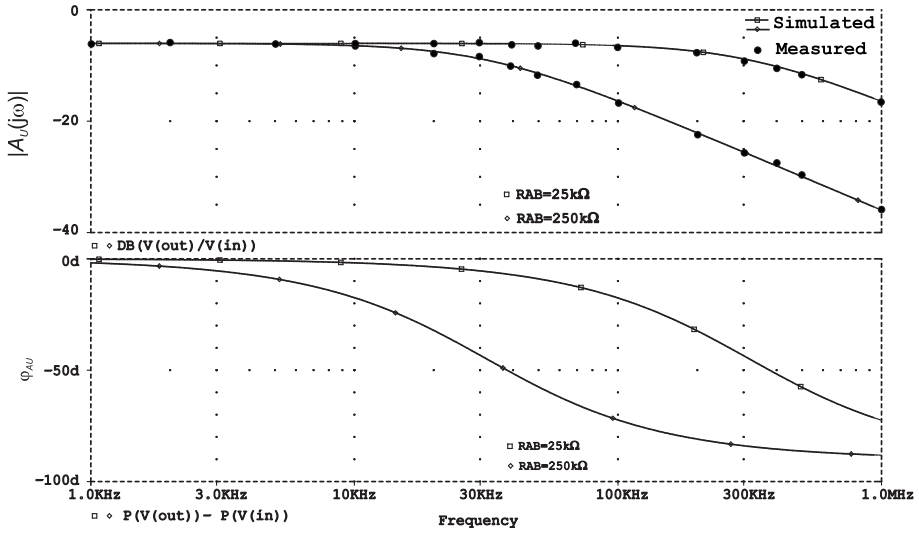

Fig. 7. Comparison of the simulation and experimental results for the programmable voltage divider.

In d.c. mode of operation of the non-inverting amplifier the output offset was checked for the values of digital code D chanced to 256, 512 and 768, the corresponding values of u_{error} according to (7) were found to be $1.46mV$, $2.76mV$ and $4.1mV$ respectively. The simulated values of the output offset are close to the calculated values and the error is not greater than 1%. The concrete values of the offsets, obtained from the experimental study are: $1.25mV$, $2.12mV$ and $3.85mV$. Moreover, an error of 10…15% between experimental and simulation results is quite acceptable considering the tolerances of the technological parameters of the chosen op amp. By increasing the temperature from $25°C$ to $55°C$ for an experimental circuit implemented on a separate FR4 PCB laminate with SMD passive components the output offset decreases from $2.12mV$ to $1.85mV$. The corresponding calculated values of this parameter from (8) are changed from $2.76mV$ to $2.08mV$.

The simulation and experimental results for the a.c. transfer characteristics at three values of the d.c. voltage gain of the non-inverting amplifier are plotted on Fig. 8. As can be seen for low frequencies approximately up to $20kHz$ the gains are with constant value and is frequency independent. At voltage gains equal to 7.25 (D = 256) and 13.5 (D = 512) in the form of the frequency response causes peaking ($Q_p > 0.707$). Moreover at gains 7.25 and 13.5, the phase shift is $\geq 90°$. For the voltage gain equal to the 19.7 (at D = 768) the calculated values by (11), (12) and (13) are $f_p = 114.3kHz$, $f_z = 161.3kHz$ and $Q_p = 0.739$. The frequency response has a small peak, due to the additional parasitic poles of the op amp. The calculated bandwidth by (16) is $157kHz$, the simulated value is $168kHz$ and the experimental result is $165kHz$, respectively. The phase margin for the three gains is greater than 45°, which means that the amplifiers are stable according to the Bode criterion [12]. The difference between the simulation and experimental results is due to the influence of the additional parasitic poles determined by the inertial properties of the op amp.

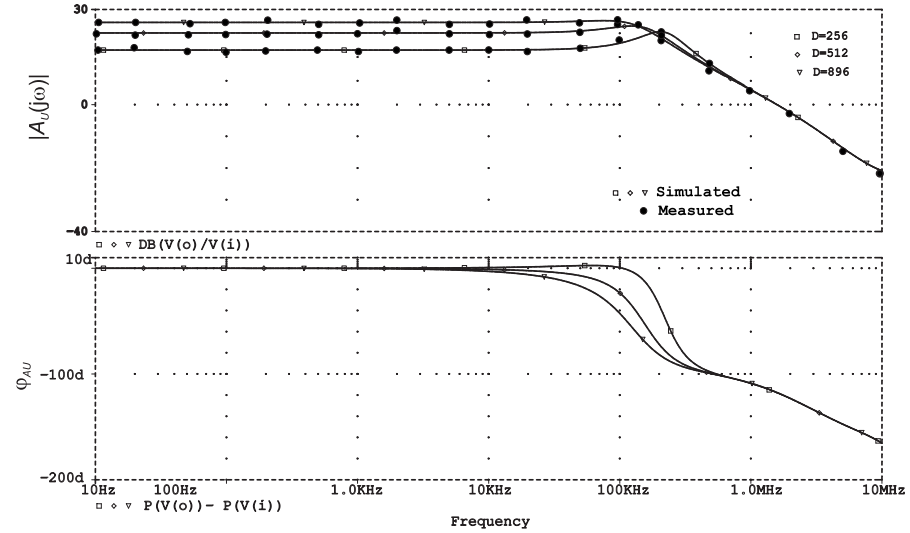

Fig. 8. Comparison of the simulation and experimental results for the programmable non-inverting amplifier circuit.

V. Conclusion

Theoretical analyses of the structure and the principal of operation of the basic programmable electronic circuits employing CMOS RDAC potentiometers have been presented. Based on the analysis are obtained equations for the transfer functions and formulas for the most important dynamic parameters. Moreover, using the obtained formulas is developed an improved macro-model of RDAC potentiometers, based on the elements and primitives from the standard ABM library build in PSpice A/D simulators. The proposed model is defined as a hierarchical block in OrCAD® Capture and accurately describes the behavior of most common digital pots, including the basic electrical parameters and some of the second-order effects such as nonlinear increment/decrement of the wiper, common-mode leakage current, noise density and temperature coefficient.

One of aims of the further work is focused on creating a VHDL-AMS – based model of digital pots, in which by the control data-word are reflected the various modes of operation of the real devices.

Acknowledgment

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Ivailo M. Pandiev was born in Sofia, Bulgaria, in 1971. He received the B.S. and M.S. degrees in electronic and automation engineering from the Technical University of Sofia, Bulgaria in 1996 and the Ph.D. degree in electronic engineering from the same university, in 2000.

Since 2001 to 2004, he was an assistant professor with the Analog electronic laboratory. Since 2005, is an associate professor with the Electronic engineering department, Technical University of Sofia, Bulgaria. Main fields of educational and scientific activities: analog electronics, mixed-signal systems employing programmable ICs (FPGA and FPAA) and behavioral modeling of electronics components and devices, using VHDL and VHDL-AMS. Books: Monography „PSpice macro-models of operational amplifiers" (2000); „Analog electronics" (2003, 2008); „Electronics devices" (2004); „Electronics and micro-processing systems" (2006); „Analog and digital electronics" (2009) and „Mixed-signal circuits and systems" – lecture notes (2012). At 2012 his monography entitled „Electronic circuits with operational amplifiers – analysis and design" has been published.