

# A 65 nm CMOS Resistorless Current Reference Source with Low Sensitivity to PVT Variations

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**Abstract**—This paper<sup>1</sup> describes a resistorless current reference source, e.g. for fast communication interfaces. Addition of currents with opposite temperature coefficient (PTC and NTC) and body effect have been used to temperature compensation. Cascode structures have been used to improve the power supply rejection ratio. The reference current source has been designed in a GLOBALFOUNDRIES 65 nm technology. The presented circuit achieves 59 ppm/°C temperature coefficient over range of -40°C to 125°C. Reference current susceptibility to process parameters variation is  $\pm 2.88\%$ . The power supply rejection ratio without any filtering capacitor at 100 Hz and 10 MHz is lower than -142 dB and -131 dB, respectively.

**Index Terms**—current reference, 65 nm CMOS, body effect, power supply circuits, threshold voltage.

## I. INTRODUCTION

CURRENT reference sources are very important parts of analog or mixed-signal integrated circuits such as PLLs, digital-to-analog and analog-to-digital converters, operational amplifiers and other devices produced nowadays and used for example in fast communication. The listed circuits require very well-defined bias current. Moreover, generated current must be independent from variation of technology process, supply voltage and temperature. Furthermore, current reference generator can be responsible for the work of the other blocks, so it should be an autonomous circuit and begin work when the voltage supply is switched on.

The current reference source presented here consists of MOSFETs and vertical p-n-p bipolar transistors. It is designed for 3.3 V supply voltage with low sensitivity to process variation and small temperature coefficient.

The paper is organized in the following way: Section II presents the known solutions of current reference circuits. The operating principles of the presented current reference source and circuit description are given in Section III. Section IV gives design considerations and simulation results. Finally, conclusions are presented in Section V.

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<sup>1</sup> Portions of this paper have been published in [7]

## II. KNOWN CIRCUITS

Current reference circuits are usually based on conception, which assumes generating two currents [1]. One of them has positive temperature coefficient (PTC), the second has negative temperature coefficient (NTC). Both of them have the same value of temperature coefficient and are added in another section of the circuit. Therefore, it is possible to obtain temperature independent output current. PTC current can be generated by a bipolar transistor but this solution needs more fabrication steps and lithographic masks. The second way is based on MOSFET transistors working in subthreshold region [2, 3]. Unfortunately, in this solution fluctuation of threshold voltage caused by process variation can be very large and may result in significant output current variation. NTC current is commonly acquired using the difference of MOSFETs threshold voltage. It is possible to obtain this difference by using another type of MOSFET transistor, e.g. with thick gate oxide [1], or by basing generation on body effect [3] which causes increase of the absolute value of threshold voltage with increase of reverse bias of S-B junction.

Other current references are based on generation of two currents with the same, positive and linear temperature coefficient but with other value of amplitude [4]. Reference current is obtained by current subtraction. If generated currents have also the same and linear dependence of supply voltage, the discussed effect makes it possible to obtain simultaneously reference current ( $I_{ref}$ ) independent of supply.

Other types of all-MOSFET current reference are based on zero temperature coefficient (ZTC) point [5, 6]. In subthreshold region dominates current of diffusion, and drain current has positive temperature coefficient. In strong inversion drain current has negative temperature coefficient. Slightly over threshold voltage occurs gate-source voltage value for which listed effects are balanced. Temperature coefficient at this point equals zero. The problem with this idea is that the ZTC point is located near threshold voltage, thus it is difficult to keep transistor over subthreshold region in all technology process corners.

## III. PROPOSED CURRENT REFERENCE CIRCUIT

The schematic diagram of proposed current source circuit is shown in Fig. 1.

That circuit generates two currents: PTC current  $I_1$  and NTC current  $I_2$ . Such currents are mirrored and added. Temperature independence is achieved by obtaining appropriate

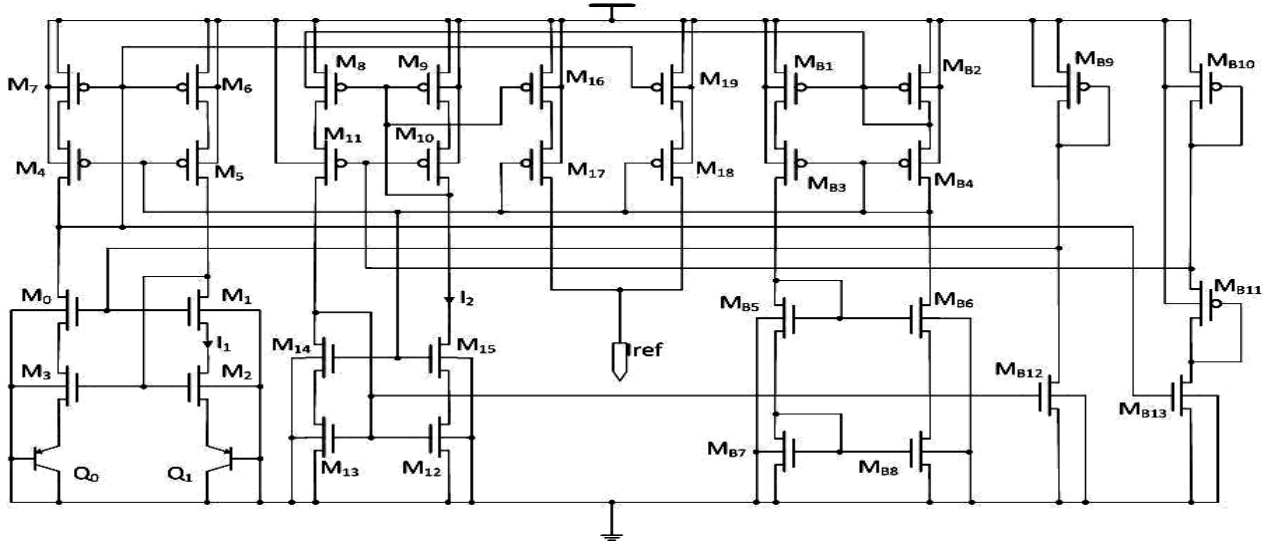


Fig. 1. Proposed current reference source.

temperature coefficient of the summed currents. Low sensitivity to supply voltage bases on using “high swing” cascode structures. Transistors  $M_{B1}-M_{B13}$  form bias block which provide bias voltage to cascode structures and bulk node of  $M_8$ . Moreover, transistors  $M_{B9}-M_{B13}$  work as start-up circuit.

All MOSFETs are 2.5 V tolerant, but with sufficiently large L they can support 3.3 V supply.  $Q_0$  and  $Q_1$  are vertical bipolar p-n-p transistors.

#### A. PTC Generator

Two bipolar p-n-p transistors  $Q_0$  and  $Q_1$ , working in diode connection, are the core of PTC current generator. Apart from them that part of circuit contains MOSFETs  $M_0-M_7$ , which operates in saturation region, where following relations apply:

$$V_{GS} = V_{TH} + \sqrt{2I_D * \frac{1}{\mu C_{OX}} * \frac{L}{W}} \quad (1)$$

and

$$V_{BE} = V_T \ln(I_C / I_S) \quad (2)$$

where  $V_{TH}$  is threshold voltage,  $\mu$  is the mobility of electrons or holes,  $C_{OX}$  is the gate oxide capacitance,  $I_C$  is collector current,  $I_S$  is saturation current of bipolar transistor,  $V_T$  is the thermal voltage and it is equal to  $kT/q$ , where  $k$  is the Boltzmann constant and  $q$  is magnitude of the electrical charge on the electron. From Kirchhoff's law we have:

$$V_{BE0} + V_{GS3} = V_{BE1} + V_{GS2}. \quad (3)$$

By substituting (1) and (2) into (3) and assuming that  $I_{M3}=I_{M2}$  we get:

$$I_1 = \frac{\mu C_{OX}}{2} * \frac{\left( \frac{kT}{q} \ln(A_{E0} / A_{E1}) \right)^2}{\left( \sqrt{L_3 / W_3} - \sqrt{L_2 / W_2} \right)^2} \quad (4)$$

where  $A_{E0}$  and  $A_{E1}$  are areas of emitter  $Q_0$  and  $Q_1$  respectively. Mobility  $\mu$  is proportional to  $T^{3/2}$  thus  $I_1$  is proportional to  $T^{1/2}$  and its derivative with respect to  $T$  is expressed by:

$$\frac{dI_1}{dT} = \frac{\mu C_{OX} k^2 T \ln^2(A_{E0} / A_{E1})}{q^2 \left( \sqrt{L_3 / W_3} - \sqrt{L_2 / W_2} \right)^2}. \quad (5)$$

#### B. NTC Generator

The NTC current generator is formed by transistors  $M_8-M_{15}$ . Current generation is based on threshold voltage difference between  $M_8$  and  $M_9$ . This difference is obtained by using body effect. Following relations apply:

$$V_{TH} = V_{TH0} + \Delta V_{TH}, \quad (6)$$

$$\Delta V_{TH} = \gamma \left( \sqrt{2|\varphi_F| + V_{SB}} - \sqrt{2|\varphi_F|} \right), \quad (7)$$

$$\gamma = \frac{\sqrt{2q\epsilon_0 k_{Si} N}}{C_{OX}} \quad (8)$$

where  $\varphi_F$  is surface potential,  $\epsilon_0$  is the permittivity of silicon,  $N$  is doping concentration,  $k_{Si}$  is relative permeability of silicon. The threshold voltage of PMOS transistor is negative, therefore if potential on bulk node of  $M_8$  is less than supply voltage its threshold voltage increases (absolute value of  $V_{TH8}$  decreases).

The drain currents of transistors in that part of the circuit are given by:

$$I_{D8} = \frac{\mu C_{OX}}{2} * \frac{W_8}{L_8} * (V_{GS} - V_{TH8})^2, \quad (9)$$

$$I_{D9} = \frac{\mu C_{OX}}{2} * \frac{W_9}{L_9} * (V_{GS} - V_{TH9})^2 \quad (10)$$

where  $V_{GS}=V_{GS8}=V_{GS9}$ . By calculating  $V_{GS}$  from (10) and substituting it in (9) the expression of the NTC current is given by:

$$I_2 = \frac{\mu C_{OX} W_8 W_9 (V_{TH8} - V_{TH9})^2}{2(\sqrt{L_8 W_9} - \sqrt{L_9 W_8})^2}. \quad (11)$$

The threshold voltage can be shown as:

$$V_{TH} = V_{FB} + \frac{\sqrt{4\varepsilon_0 k_s q N \varphi_F}}{C_{OX}} + 2\varphi_F \quad (12)$$

where  $V_{FB}$  is the flat band voltage,  $\varphi_F$  is the surface potential and it is given by:

$$\varphi_F = \frac{kT}{q} \ln\left(\frac{N}{n_i}\right). \quad (13)$$

In this relationship  $n_i$  is the intrinsic doping value and its temperature variation can be expressed by:

$$n_i(T) = AT^{3/2} \exp\left(\frac{-E_{g0}}{2kT}\right) \quad (14)$$

where  $A$  is the temperature coefficient and  $E_{g0}$  is the band gap energy of silicon. By substituting (12) and (13) into (11), and calculating NTC current derivative with respect to  $T$ , it is possible to note that this derivative is negative.

### C. Summation of Currents

The current summing block consists of transistors  $M_{16}$ - $M_{19}$ . In this part reference current is obtained by adding currents with opposite temperature coefficient. The output current can be shown as:

$$I_{REF} = I_1 + I_2 = \frac{\mu C_{OX}}{2} * \frac{\left(\frac{kT}{q} \ln(A_{E0}/A_{E1})\right)^2}{\left(\sqrt{L_3/W_3} - \sqrt{L_2/W_2}\right)^2} + \frac{\mu C_{OX} W_8 W_9 (V_{TH8} - V_{TH9})^2}{2(\sqrt{L_8 W_9} - \sqrt{L_9 W_8})^2}. \quad (15)$$

This relation shows that with carefully designed emitter areas ratio of bipolar transistors and channels dimensions of MOSFETs  $M_3$ ,  $M_2$ ,  $M_8$ ,  $M_9$ , a zero temperature coefficient of  $I_{REF}$  can be achieved.

## IV. SIMULATIONS RESULTS

The proposed circuit was designed for implementation in 65 nm GLOBALFOUNDRIES CMOS technology using the BSIM4.5 models, which include e.g. gate leakage current. Simulations were run in Spectre simulator.

The simulation result of output current versus temperature shows temperature coefficient of the reference current. This analysis was performed for 10% supply voltage variation and its result is demonstrated in Fig. 2. Temperature range is very wide: from  $-40^\circ\text{C}$  to  $120^\circ\text{C}$ . Temperature coefficients takes the value of 132 ppm/ $^\circ\text{C}$ , 59 ppm/ $^\circ\text{C}$  and 218 ppm/ $^\circ\text{C}$  for  $V_{DD}$  equals 2.97 V, 3.3 V and 3.63 V respectively. What is important, for narrower (but still wide) temperature range: from  $-20^\circ\text{C}$  to  $100^\circ\text{C}$ , temperature coefficient is equal to 112 ppm/ $^\circ\text{C}$ , 35 ppm/ $^\circ\text{C}$  and 157 ppm/ $^\circ\text{C}$ . These results indicate that the circuit generates stable reference current with temperature. The  $I_{ref}$  variation with presented supply changes is  $\pm 2.89\%$ .

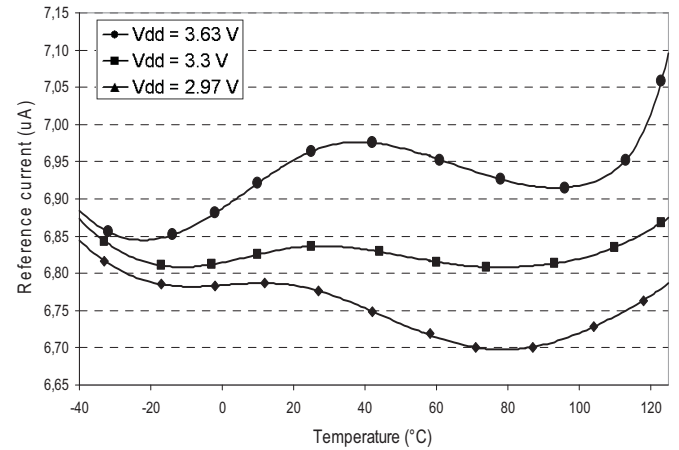


Fig. 2. The reference current versus temperature for 10% supply voltage variation.

Monte Carlo (MC) simulation was used to test the impact of the process parameters variation and transistors mismatch on the generated current. For analog circuits, MC is a better way than process corners (PC) analysis to check the influence of the mentioned effects on output current. That is because in this case PC simulation can give worse results than in reality. Moreover, reference sources are often sensitive to transistors mismatch, which is not included in PC analysis. Statistical models were used for all devices in the circuit.

The MC analysis proved that presented current reference source has very low sensitivity to the process parameters fluctuation, which is shown in Fig. 3. The mean value of  $I_{ref}$  across 1000 runs was 6.847  $\mu\text{A}$  with standard deviation of 195 nA which is 2.85% of average current. The result of the MC simulation with process variation and geometrical mismatch shows that the mean value of the output current is 6.847  $\mu\text{A}$  with standard deviation of 197 nA which is 2.88% of average value (see Fig. 4). The difference is only 0.03%, therefore the presented circuit is insensitive to dispersion of devices geometrical dimensions.

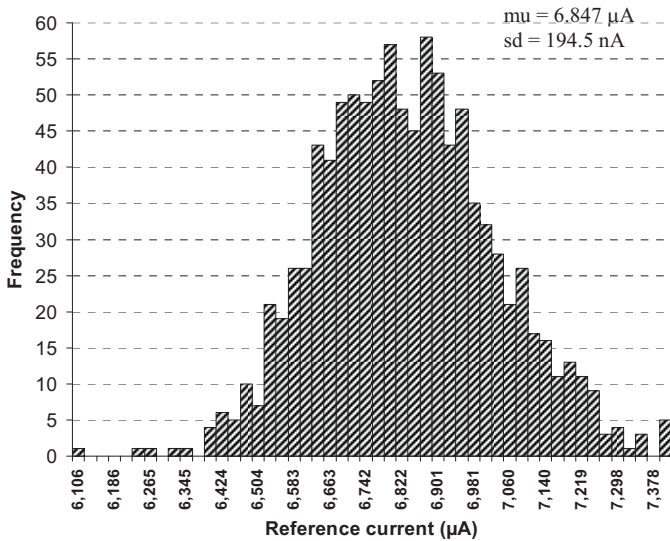


Fig. 3. Monte Carlo distribution of  $I_{ref}$  value at 27°C with dispersion in process parameters for 1000 runs.

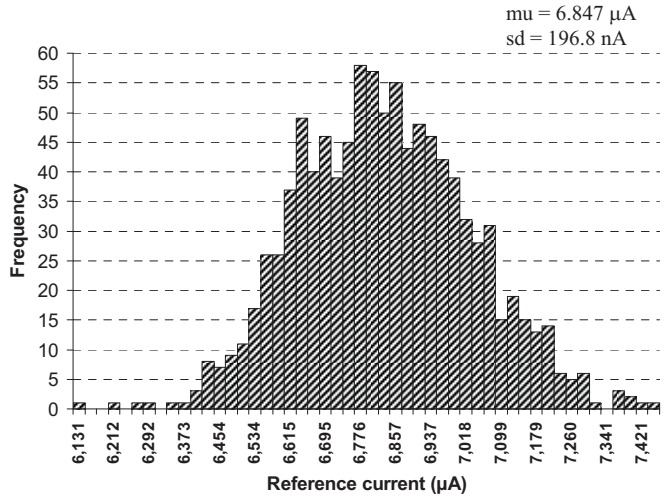


Fig. 4. Monte Carlo distribution of  $I_{ref}$  value at 27°C with dispersion in process parameters and geometrical mismatch for 1000 runs.

In GLOBALFOUNDRIES technology MOSFETs mismatch is divided into geometrical and dopant mismatch. As it was mentioned above geometrical part concerns fluctuation of transistor channel dimensions. The dopant mismatch models dispersion of number of dopant atoms, which are located in the transistor channel. This dispersion has significant impact on the reference current. As it is demonstrated in Fig. 5 the mean value of the output current is 6.851  $\mu\text{A}$  with the standard deviation of 309 nA which is 4.5% of average value.

The dispersion of distribution of channel doping is the main cause of threshold voltage fluctuation. Selective MC simulations were performed as the method to find reason of high susceptibility to dopant mismatch. All MOSFETs were checked one by one. The influence of discussed phenomenon on  $I_{ref}$  can be reduced by increasing W and L of transistors:  $M_2, M_3, M_6, M_7, M_{16}$  and  $M_{19}$ . This follows from the Pelgrom’s law, which shows that local dispersion of threshold voltage decreases with increase of square root of transistor channel area. Moreover, each dimension: W and L should be individually large enough.

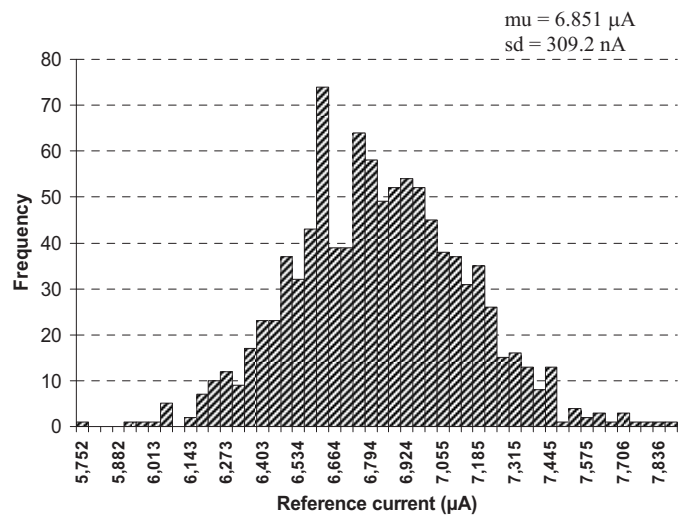


Fig. 5. Monte Carlo distribution of  $I_{ref}$  value at 27°C with dispersion in process parameters, geometrical and dopant mismatch for 1000 runs.

The MC simulation also shows that the mean value of the temperature coefficient equals 168 ppm/°C, 170 ppm/°C and 213 ppm/°C for simulation with dispersion in process parameters (PP), PP and geometrical mismatch, PP and both types of mismatch (geometrical and dopant) respectively. This analysis and results of the  $I_{ref}$  vs temperature for 10% supply voltage variations (see Fig. 2) confirm the fact that presented current reference source can be used even in that integrated circuits which require very high precision of biasing currents. This situations takes place because most of the currently produced chips is trimmed after production which aims to reduce the impact of process parameters variation. Parameters of the presented circuit ( $I_{ref}$  and temperature coefficient) has low sensitivity to devices mismatch. Therefore after trimming accuracy of the reference current should be greatly higher.

The power supply rejection ratio (PSRR) is -142 dB at 100 Hz and -131 dB at 10 MHz (see Fig. 6). The presented circuit does not contain any filtering capacitors.

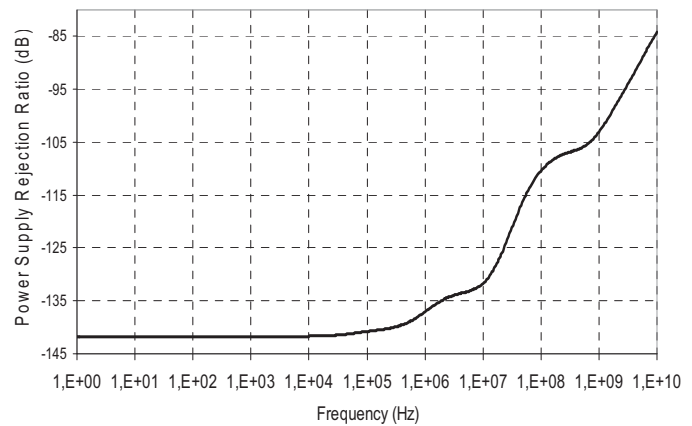


Fig. 6. PSRR simulation of the current reference circuit.

The setting time of the circuit at start-up has been evaluated around 16  $\mu\text{s}$ , 28  $\mu\text{s}$  and 167  $\mu\text{s}$  for temperature equals 125°C, 27°C and -40°C respectively. The start-up simulation is show in Fig. 7.



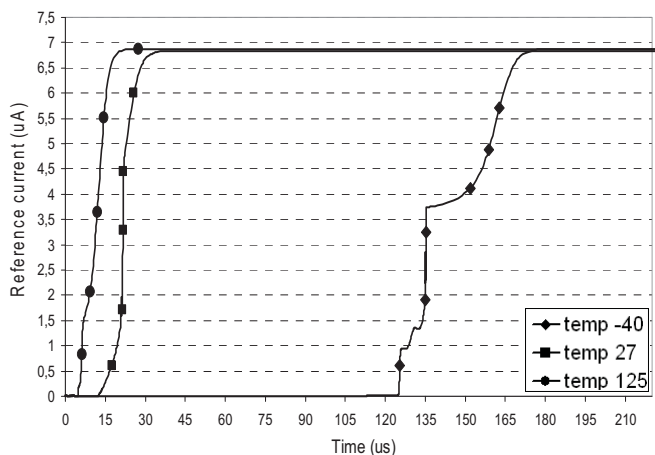


Fig. 7. Transient response at the start-up of proposed current source. Supply voltage setup time is 3.3  $\mu$ s.

Fig. 8 presents the supply voltage dependence of the reference current. The results indicate that the minimum supply voltage is 2.75 V. The  $I_{ref}$  variation in  $\pm 10\%$  supply voltage range is 0.3%, 1.4% and 2.2% for  $-40^\circ\text{C}$ ,  $27^\circ\text{C}$  and  $125^\circ\text{C}$  respectively.

TABLE I  
SUMMARY OF THE SIMULATIONS RESULTS

|                         |                       |             |
|-------------------------|-----------------------|-------------|
| Technology feature size | nm                    | 65          |
| Reference current       | $\mu\text{A}$         | 6.84        |
| Temperature coefficient | ppm/ $^\circ\text{C}$ | 59          |
| Temperature range       | $^\circ\text{C}$      | -40 / +125  |
| Process sensitivity     | %                     | 2.88        |
| Supply voltage range    | V                     | 2.75 – 3.63 |
| Current consumption     | $\mu\text{A}$         | 51          |
| PSRR @ 100 Hz           | dB                    | -142        |
| PSRR @ 10 MHz           | dB                    | -131        |

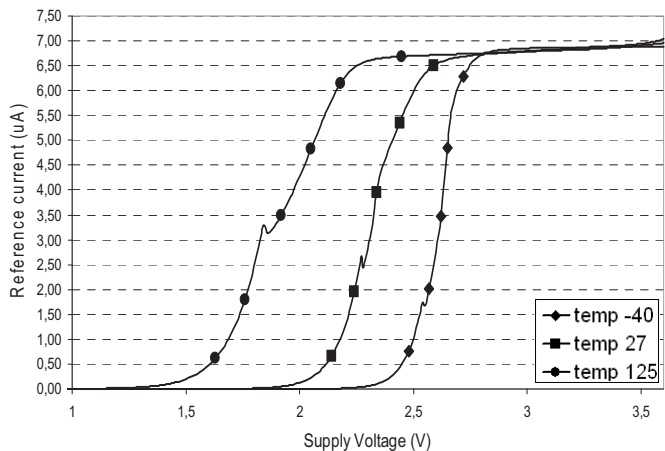


Fig. 8. The reference current as a function of supply voltage.

The layout of proposed current reference source is presented in Fig. 9. Height of the designed block is 107.08  $\mu\text{m}$  and width is 63.155  $\mu\text{m}$ , which gives area equals 0.00676  $\text{mm}^2$ .

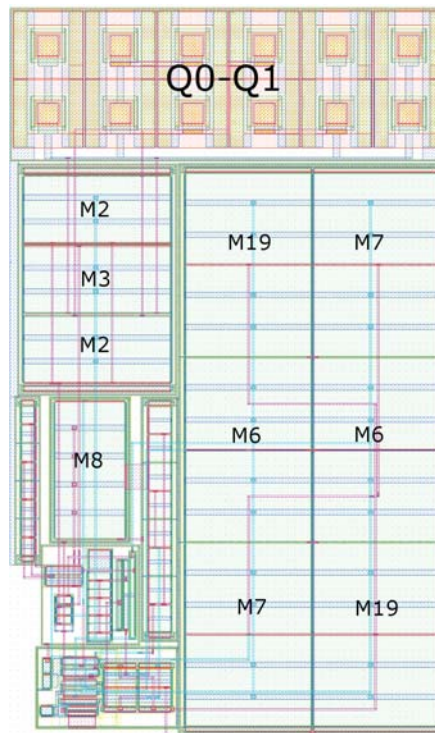


Fig. 9. The layout of designed current reference source.

TABLE II  
PERFORMANCE COMPARISON TO OTHER WORKS

|                         |                       | This work | Liu [1]   | Bendali [5] | Yoo [4]  |
|-------------------------|-----------------------|-----------|-----------|-------------|----------|
| Technology feature size | nm                    | 65        | 180       | 180         | 250      |
| Reference current       | $\mu\text{A}$         | 6.84      | 10        | 144         | 10.45    |
| Temperature coefficient | ppm/ $^\circ\text{C}$ | 59 - 218  | 170       | 185         | 60 - 720 |
| Temperature range       | $^\circ\text{C}$      | -40 – 125 | -20 – 120 | 0 - 100     | 0 – 100  |
| Process sensitivity     | %                     | 2.84      | 4.3       | 7           | ---      |
| Supply voltage range    | V                     | Min. 2.75 | 2 – 3     | Min. 1      | 1.1 – 3  |
| Current consumption     | $\mu\text{A}$         | 51.73     | ---       | ---         | 70       |

### V. CONCLUSIONS

The resistorless current reference source was presented. It obtains very promising performance. Temperature coefficient of reference current is 59 ppm/ $^\circ\text{C}$  in the temperature range between  $-40^\circ\text{C}$  and  $125^\circ\text{C}$ , which is state-of-the-art result. Moreover, sensitivity to process variations and geometrical mismatch, simultaneously, is low and takes the value of  $\pm 2.88\%$ . Influence of dopant mismatch can be reduced by increasing dimension of transistors channels. The result of PSRR analysis is very satisfactory: -142 dB at 100 Hz and -131 dB at 10 MHz, without using filtering capacitors. Achieved results show distinctly that developed architecture of current reference source can be easily used in a wide range of mixed-signal integrated circuits.

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Dr. Pleskacz has received various awards including: Ministry of National Education Award for teaching achievements in microelectronics in 1993, Ministry of Science and Higher Education Award for education achievements in microelectronics in 2006, 4 awards for scientific and teaching achievements from Rector of Warsaw University of Technology (in 1989, 1996, 2010 and 2012), and 3 *Golden Chalks* – Student Council of the Faculty Teaching Awards (in 2000, 2008 and 2012).